

# Compal Confidential

*HM51\_TR/HM70\_TR Discrete*

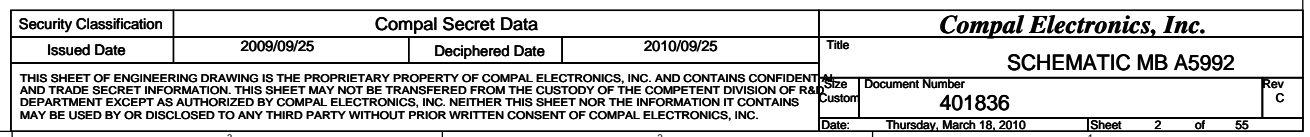
**NDWG2/NDWH1 LA5992 Schematic Document**

**Mobile AMD S1G3/RS880M/SB710**

**2009/12/02 Rev 1.0**

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**File Name : LA-5992P**



Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V HT	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

## External PCI Devices

### EC SM Bus1 address

### EC SM Bus2 address

## SB710 SM Bus 2 address

Device	Address
New Card	

## SB710 SM Bus 2 address

Device	Address
New Card	

### Board ID / SKU ID Table for AD channel

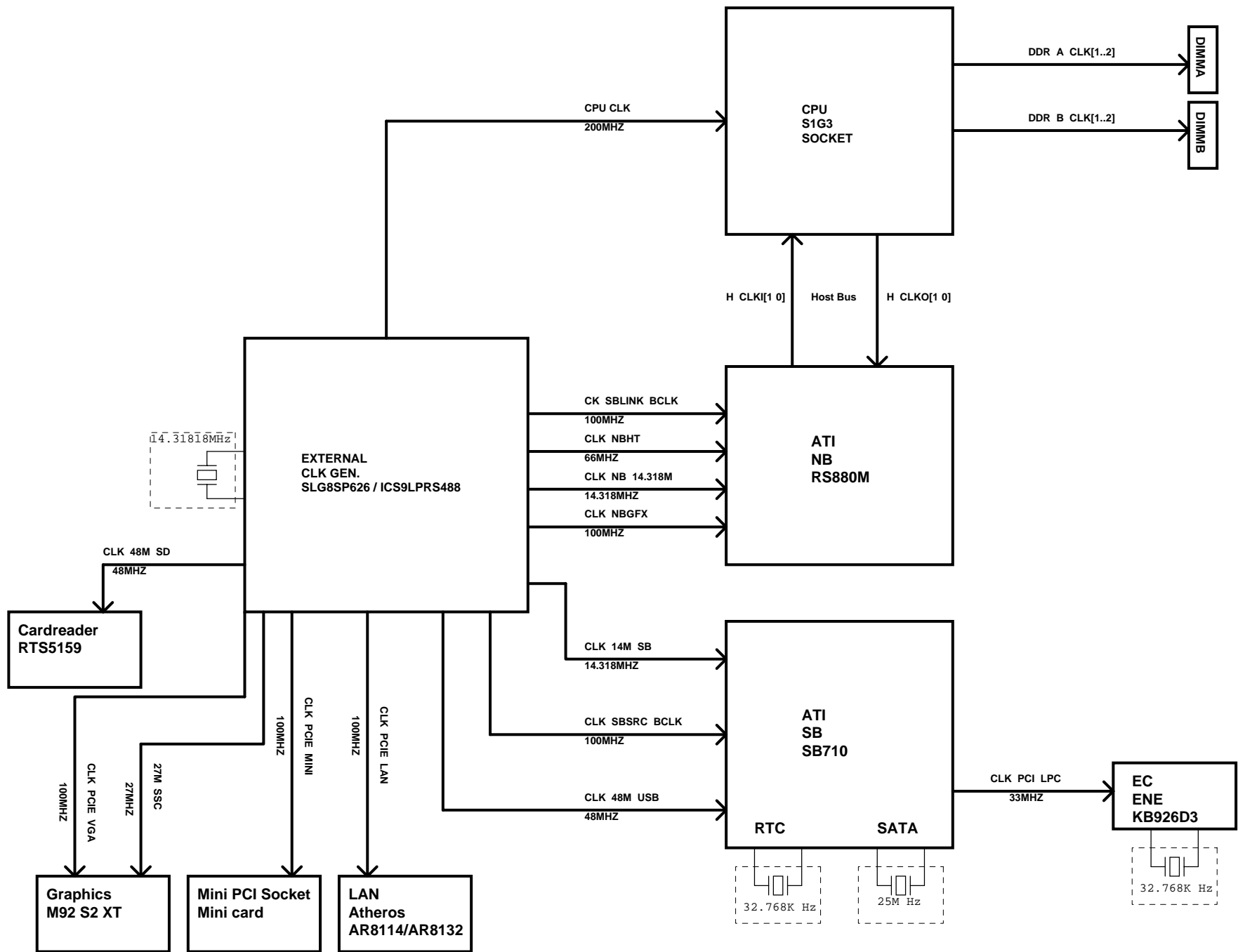
### BOARD ID Table

### BTO Option Table

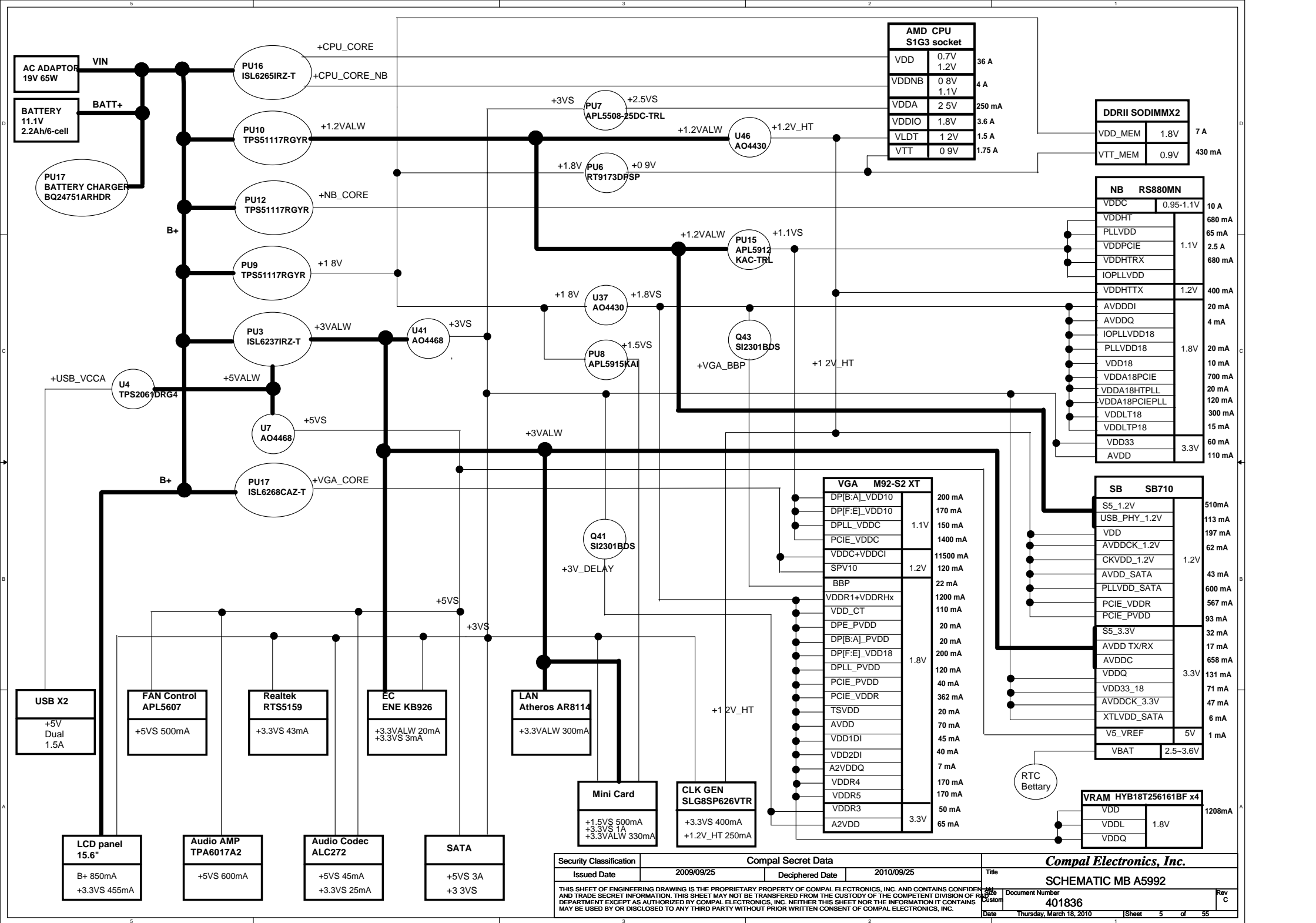
## PROJECT ID Table

SKU ID	SKU
0	NDWG2
1	
2	
3	
4	
5	
6	
7	NDWH1

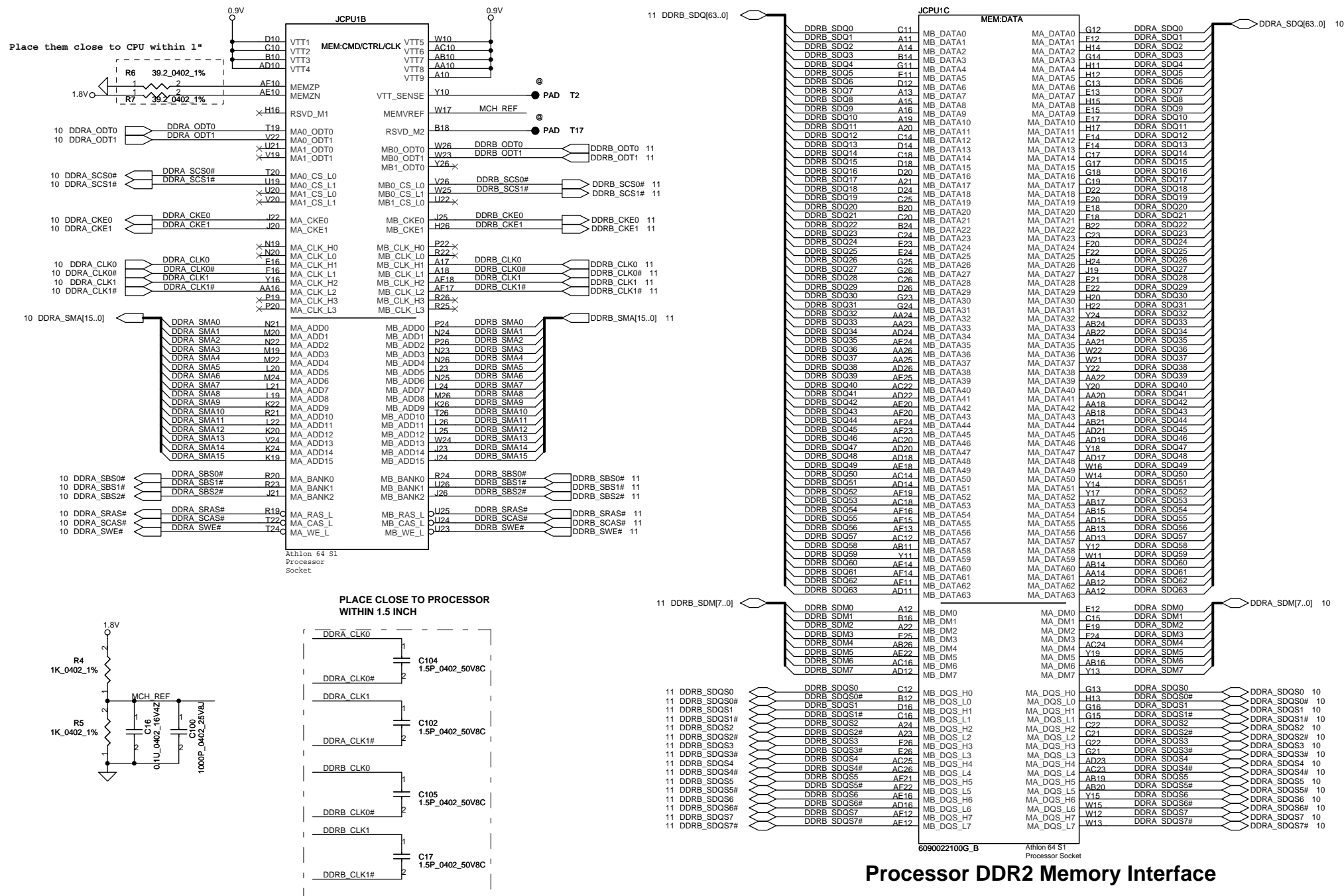
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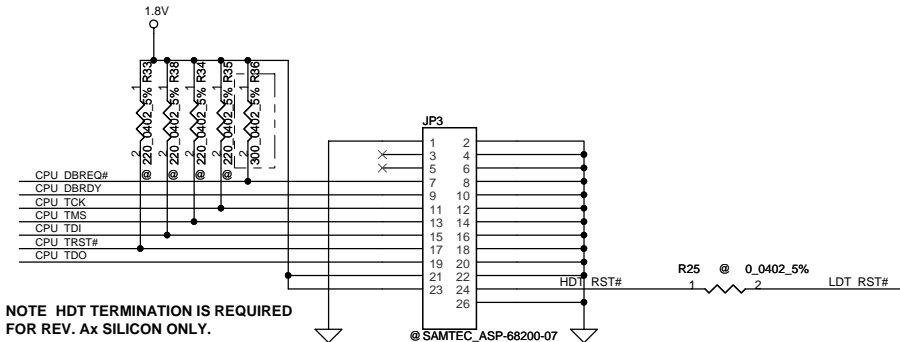
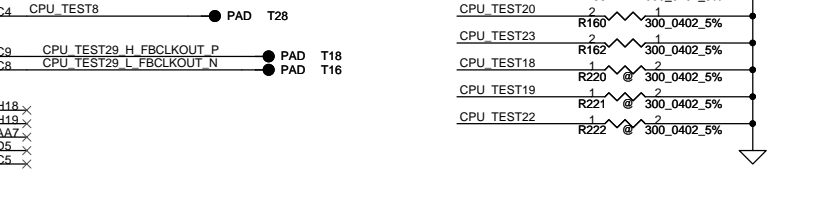
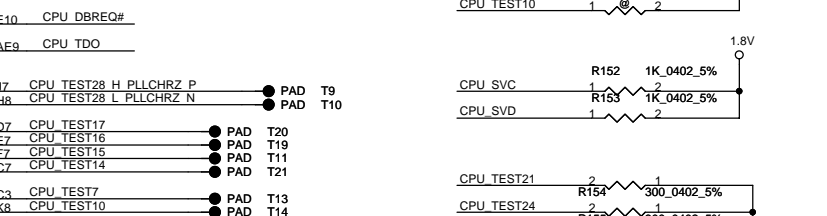
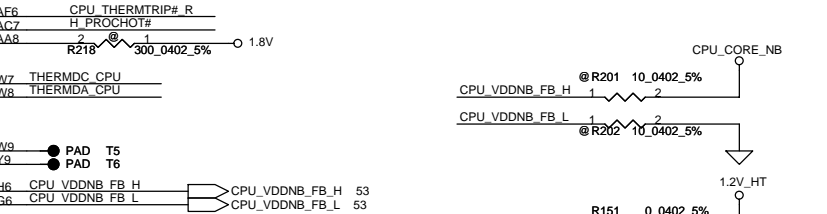
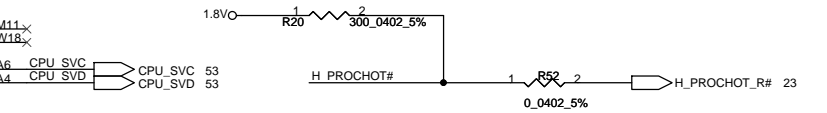
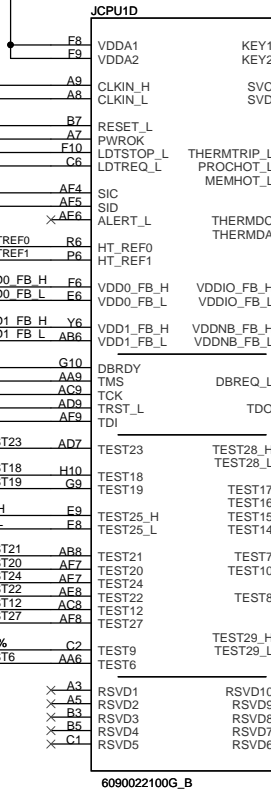
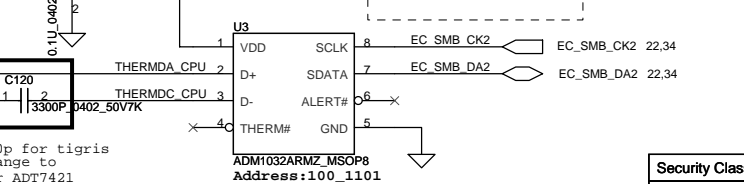
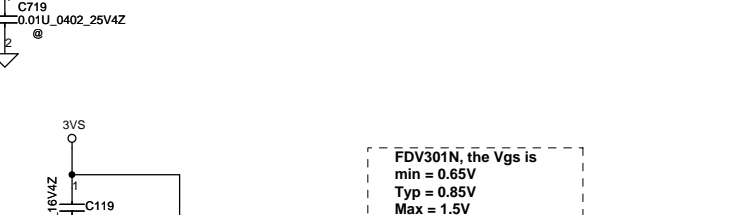
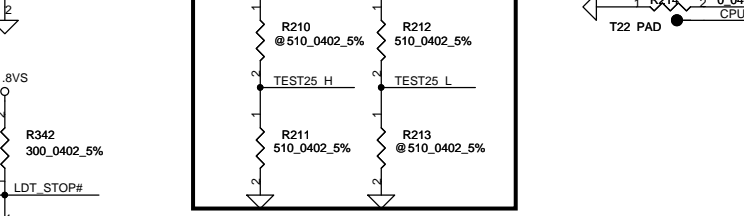
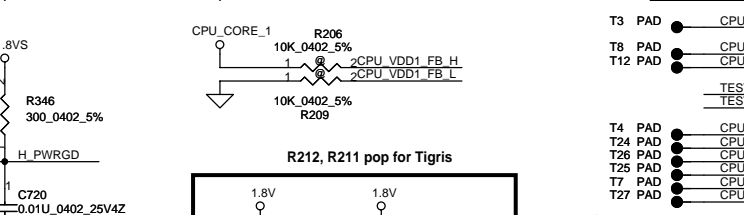
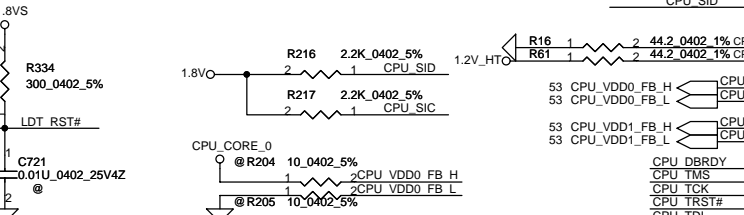
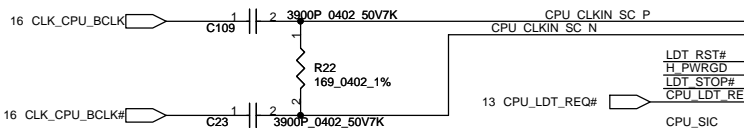
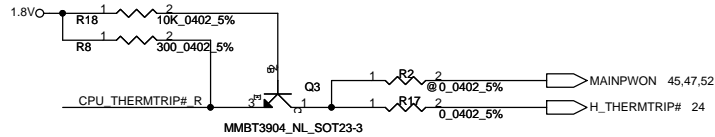
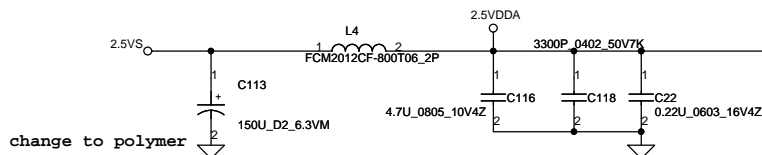


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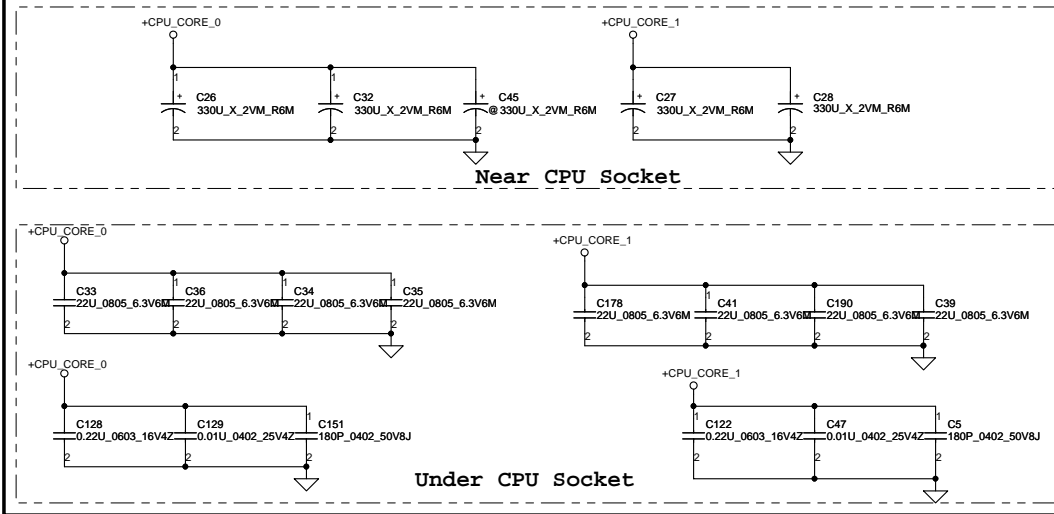


NOTE HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

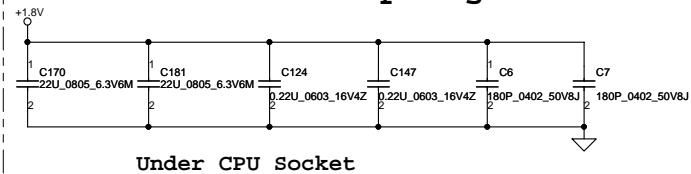
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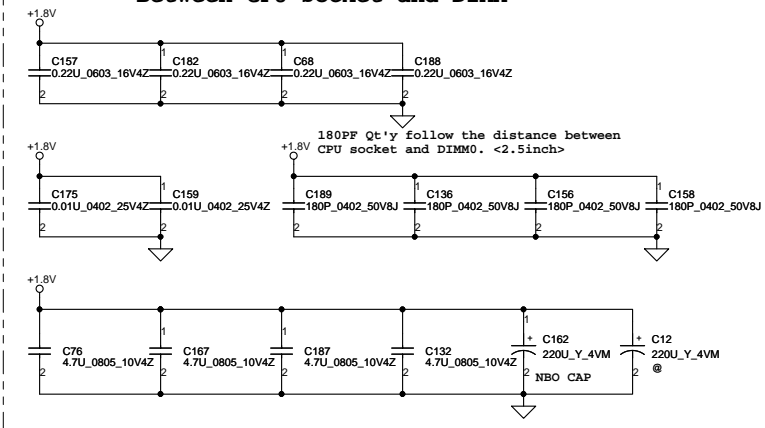
**VDD(+CPU\_CORE) decoupling.**



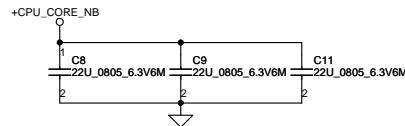
~~VDDIO decoupling.~~



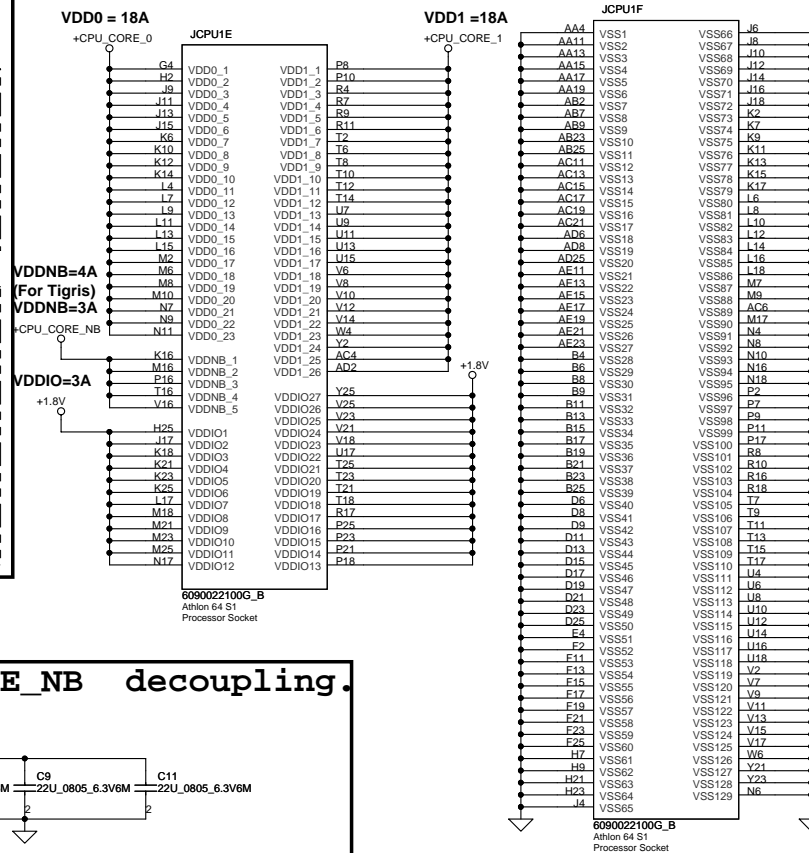
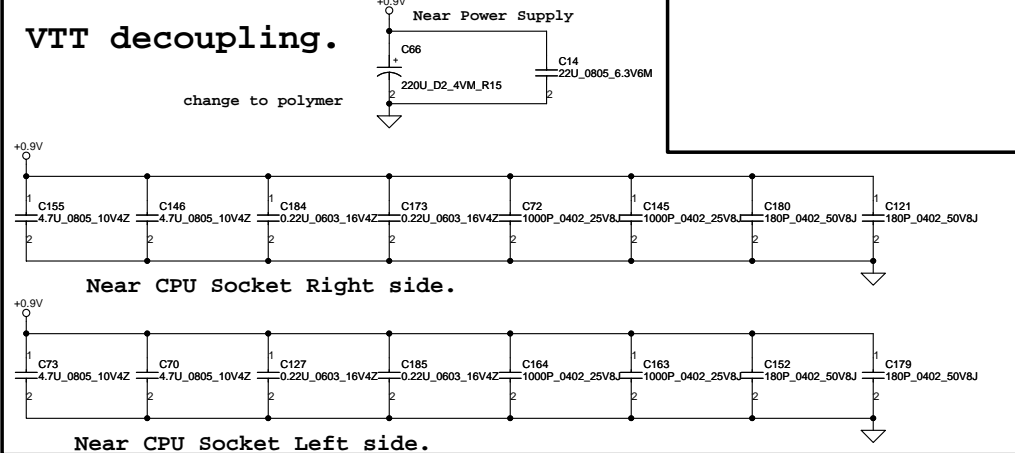
### Between CPU Socket and DIMM



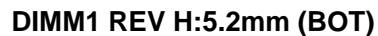
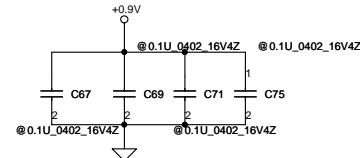
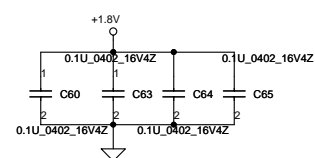
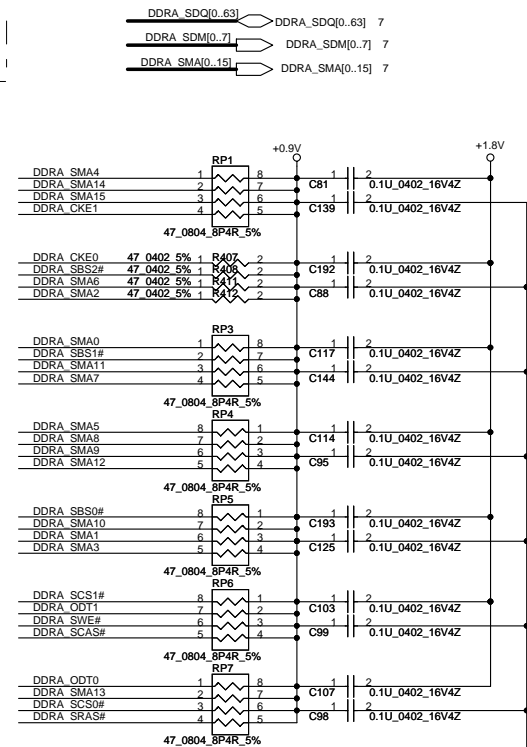
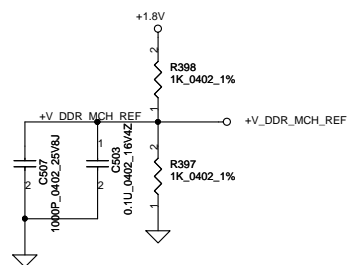
```
+CPU_CORE_NB    decoupling.
```



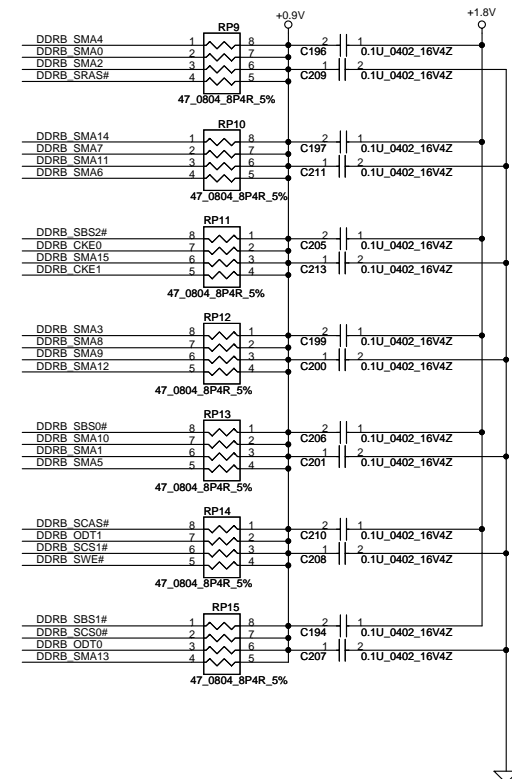
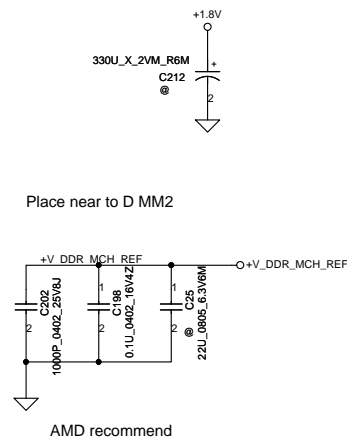
## VTT decoupling.



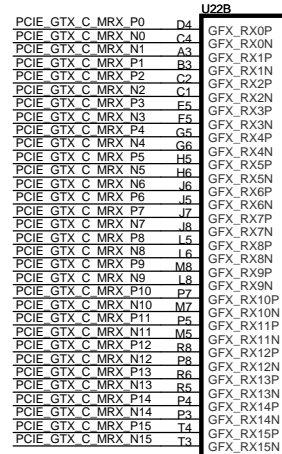
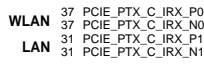
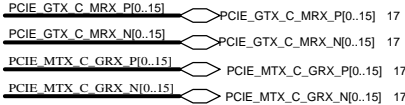
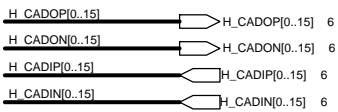
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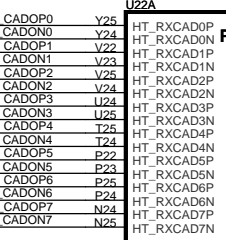
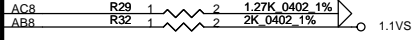
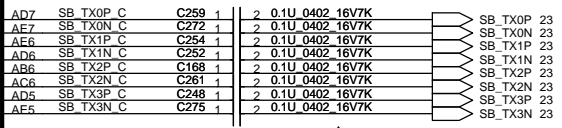
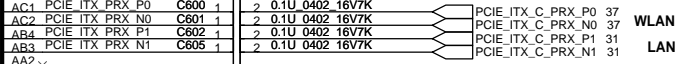
PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

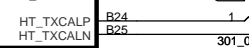
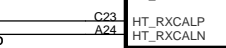
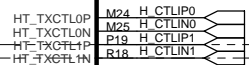
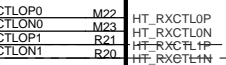
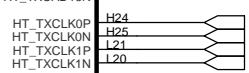
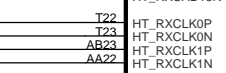
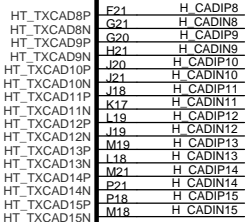
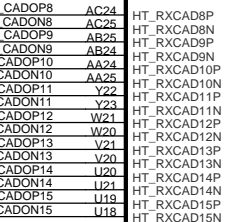
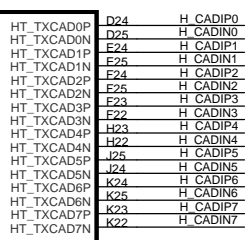
PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

RS880M\_FCBGA528



PART 1 OF 6

HYPER TRANSPORT CPU I/F



Check AMD

Place within 1" layout 4/8

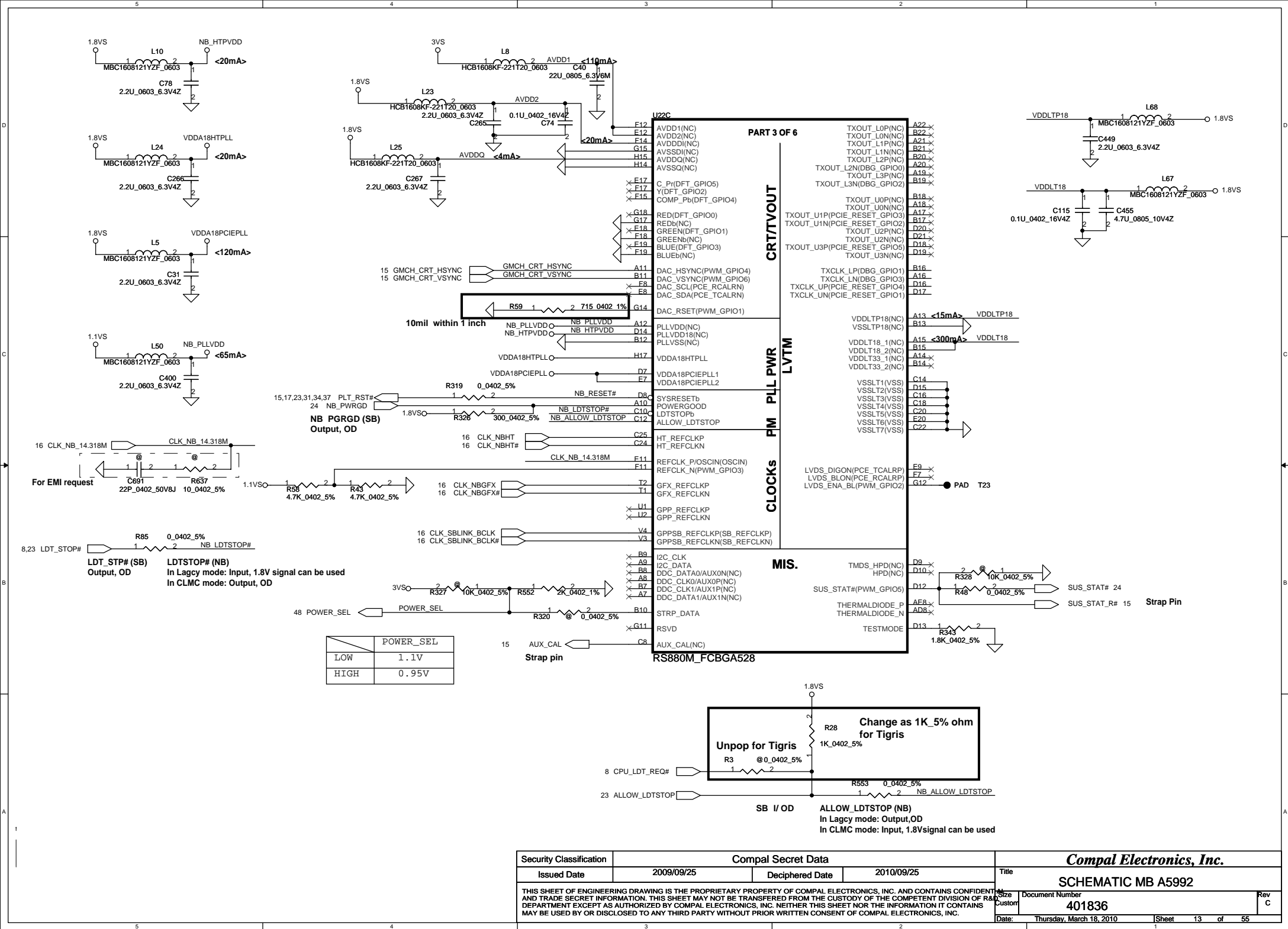
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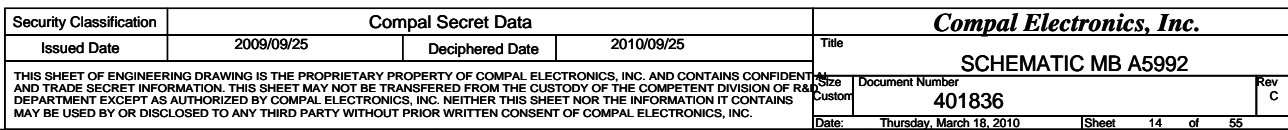
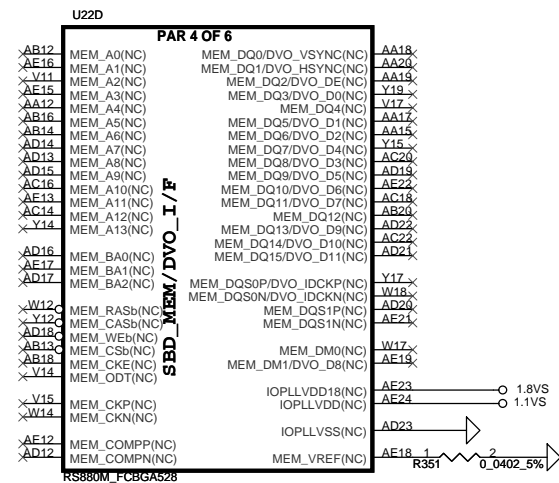
HT Link  
When tune trace length, must keep 1" on self-trace

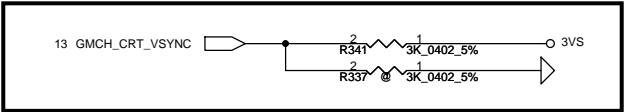
Place within 1" layout 4/8

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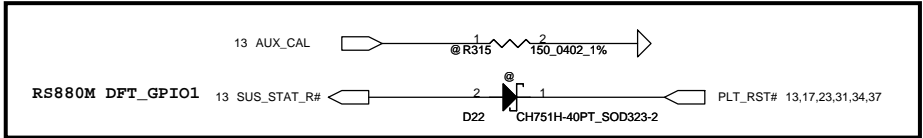






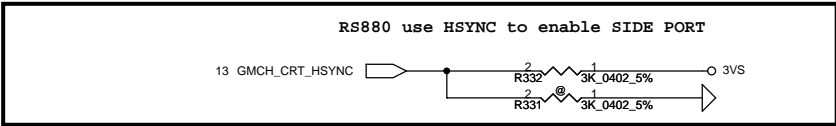
**DFT GPIO5 STRAP DEBUG BUS GPIO ENABLEd**

Enables the Test Debug Bus using GPIO. (VSYNC)  
1 : Disable (RS880)  
0 : Enable (Rs880)



**DFT GPIO1 LOAD EEPROM STRAPS**

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740/RX780/RS880M: DFT\_GPIO1 RS880M:SUS\_STAT



**RS880 use HSYNC to enable SIDE PORT**

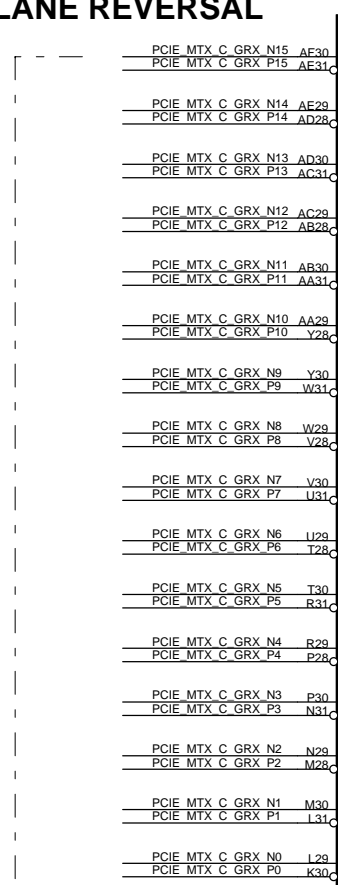
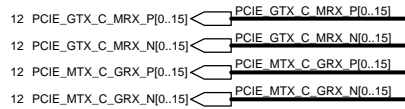
RS740/RS780/RS880M: Enables Side port memory ( RS880M use HSYNC#)  
0. Enable (RS880M)  
1 : Disable(RS880M)

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## PCIE LANE REVERSAL



U88A

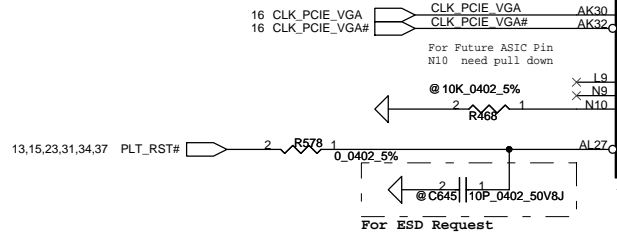
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PCIE\_RX0NPCIE\_RX1P  
PCIE\_RX1NPCIE\_RX2P  
PCIE\_RX2NPCIE\_RX3P  
PCIE\_RX3NPCIE\_RX4P  
PCIE\_RX4NPCIE\_RX5P  
PCIE\_RX5NPCIE\_RX6P  
PCIE\_RX6NPCIE\_RX7P  
PCIE\_RX7NPCIE\_RX8P  
PCIE\_RX8NPCIE\_RX9P  
PCIE\_RX9NPCIE\_RX10P  
PCIE\_RX10NPCIE\_RX11P  
PCIE\_RX11NPCIE\_RX12P  
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PCIE\_RX14NPCIE\_RX15P  
PCIE\_RX15N

PCI EXPRESS INTERFACE

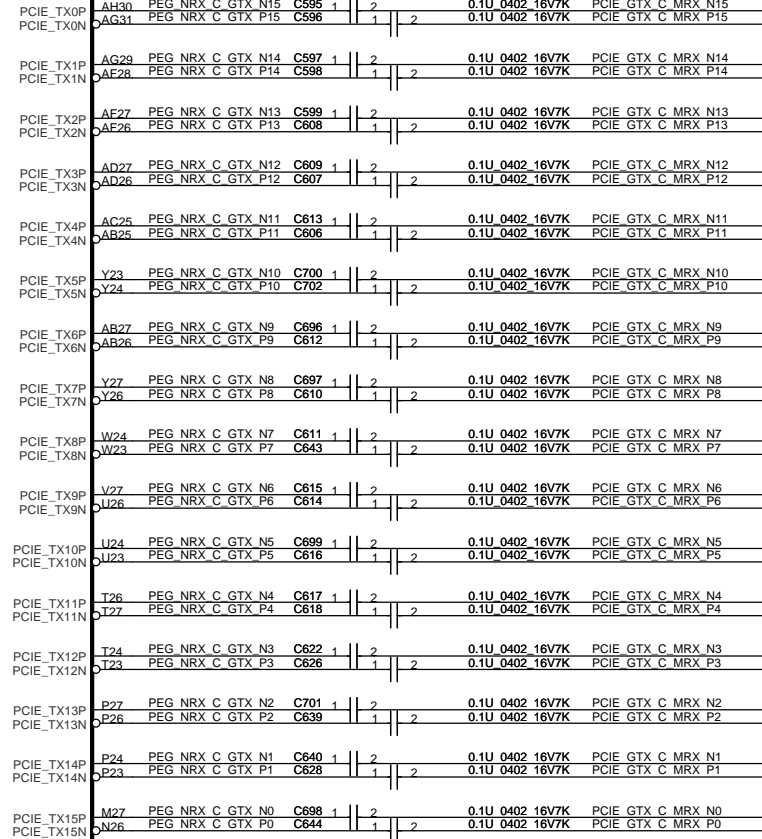
CLK  
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PCIE\_REFCLKNNC#1  
NC#2  
NC\_PWRGOOD

PERSTB

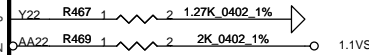
216-0728018 A12 M92-S2 XT FCBGA 0FA



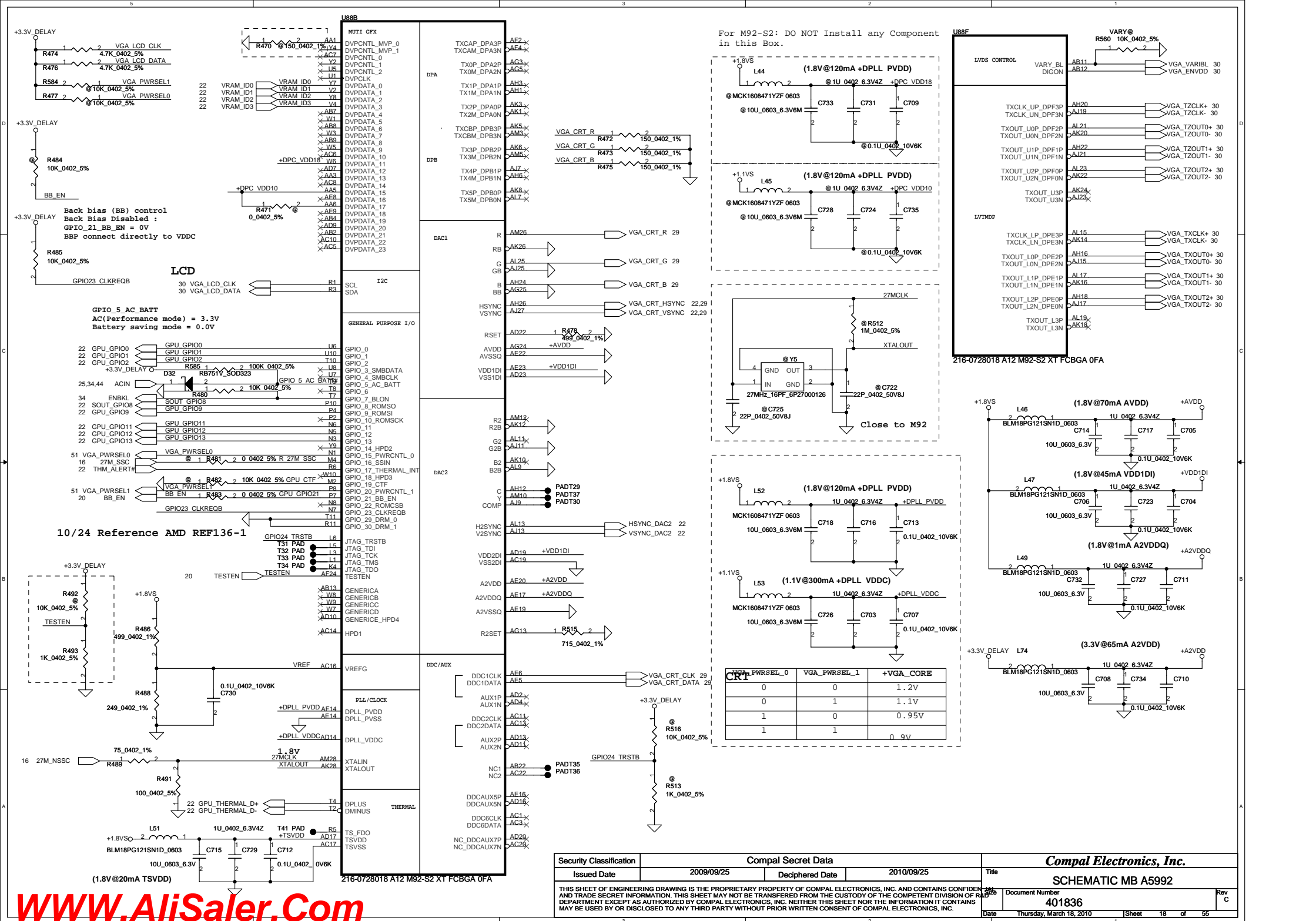
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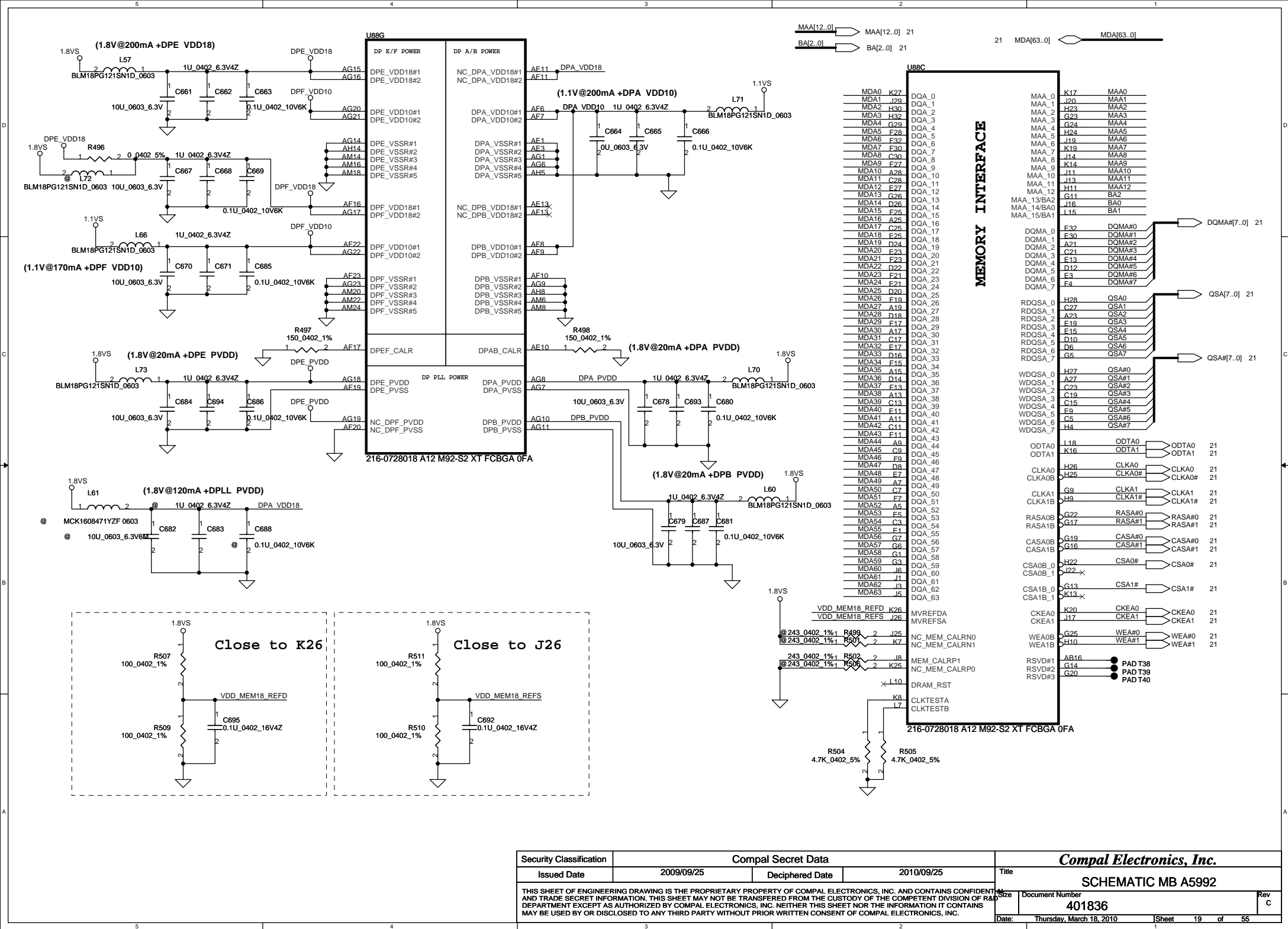


CALIBRATION

PCIE\_CALRP  
PCIE\_CALRN

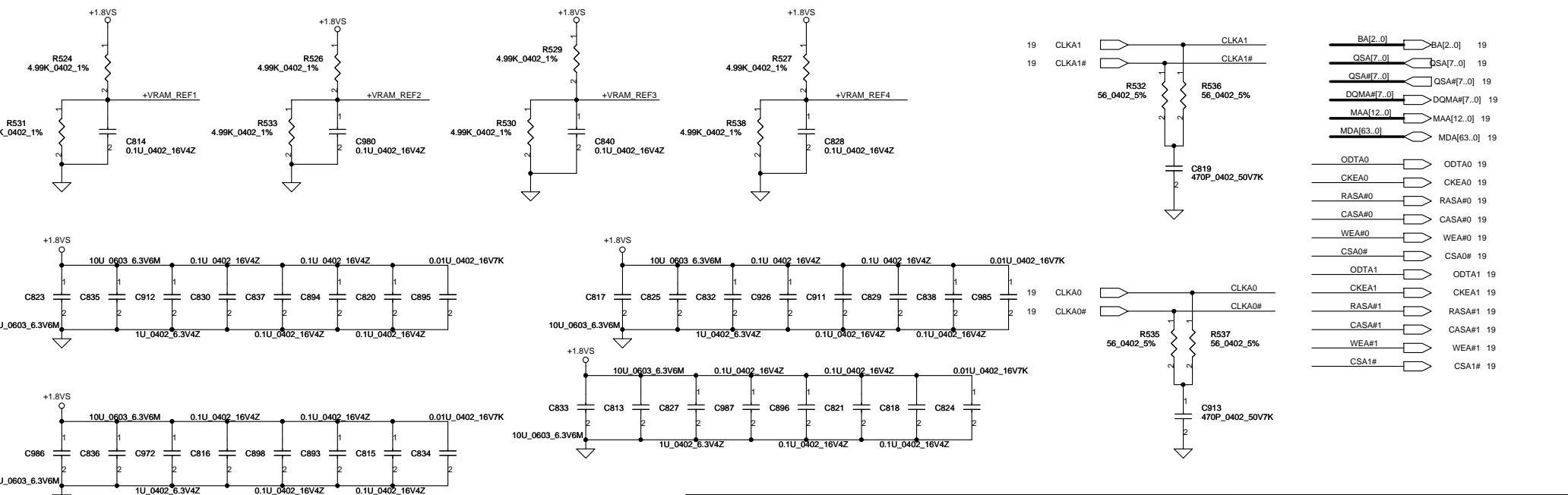
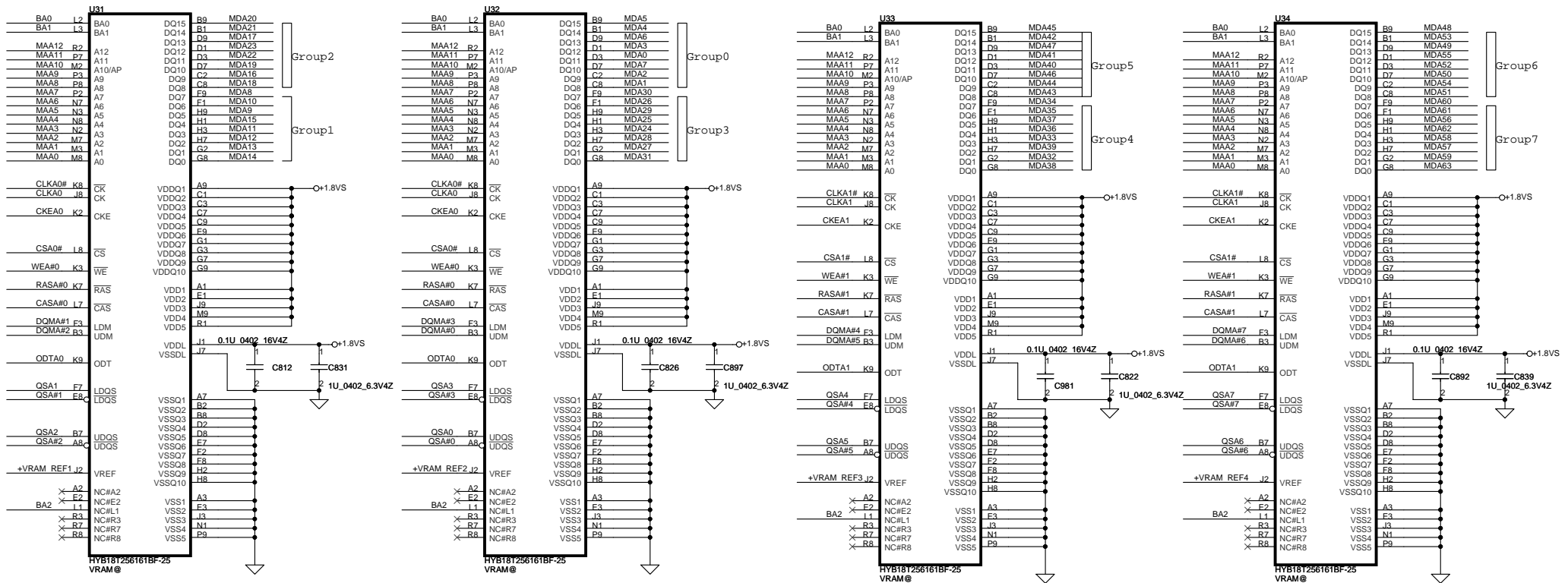
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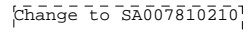
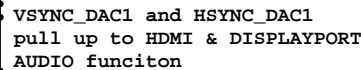
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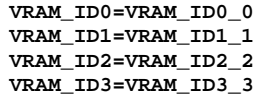


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## 3.3V\_DELAY



**Address 1001 101X b**



**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

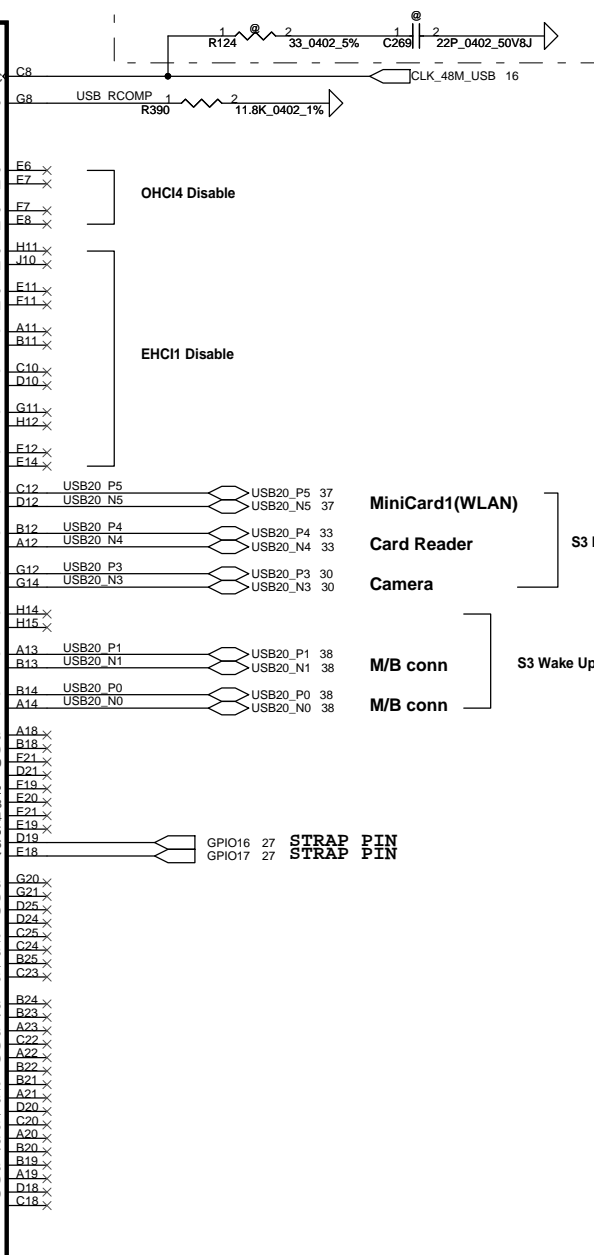
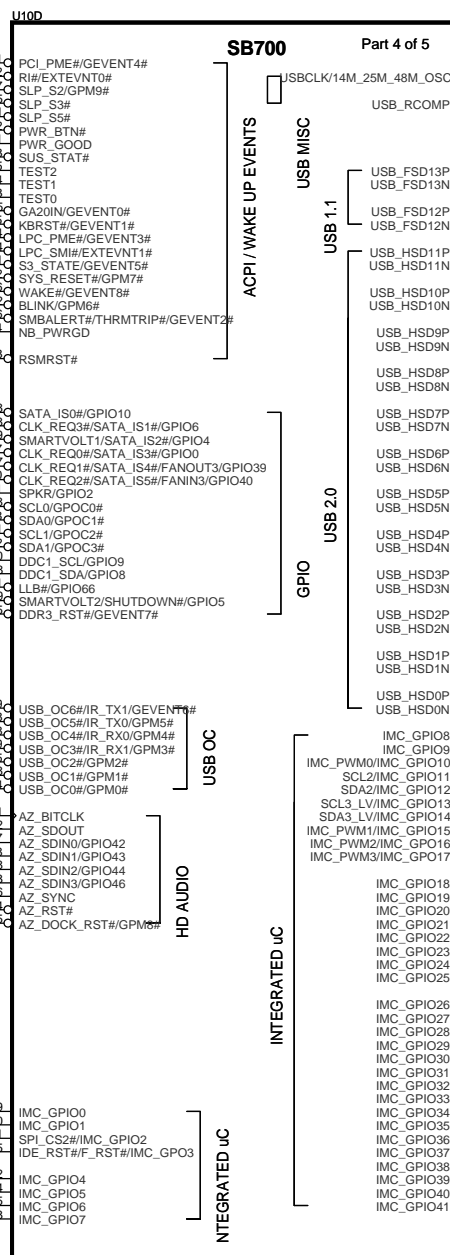
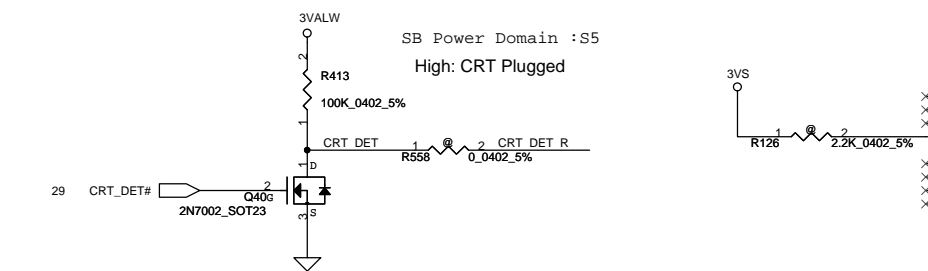
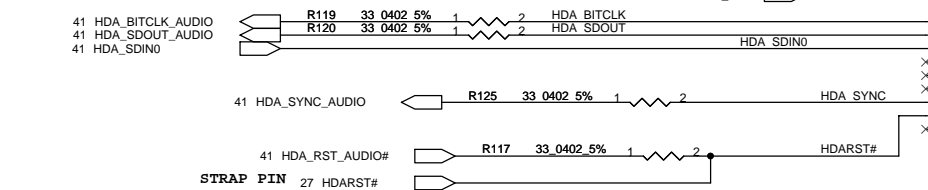
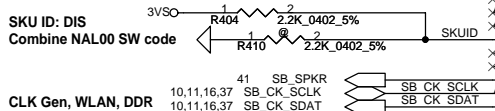
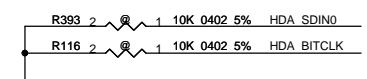
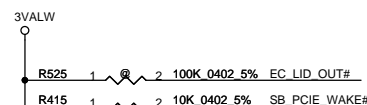
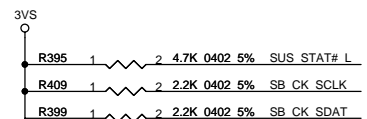
## AMD RESERVED CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

**PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

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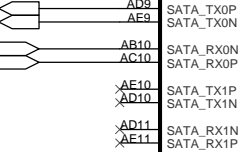
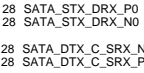
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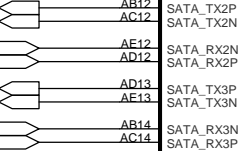
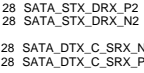


Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller

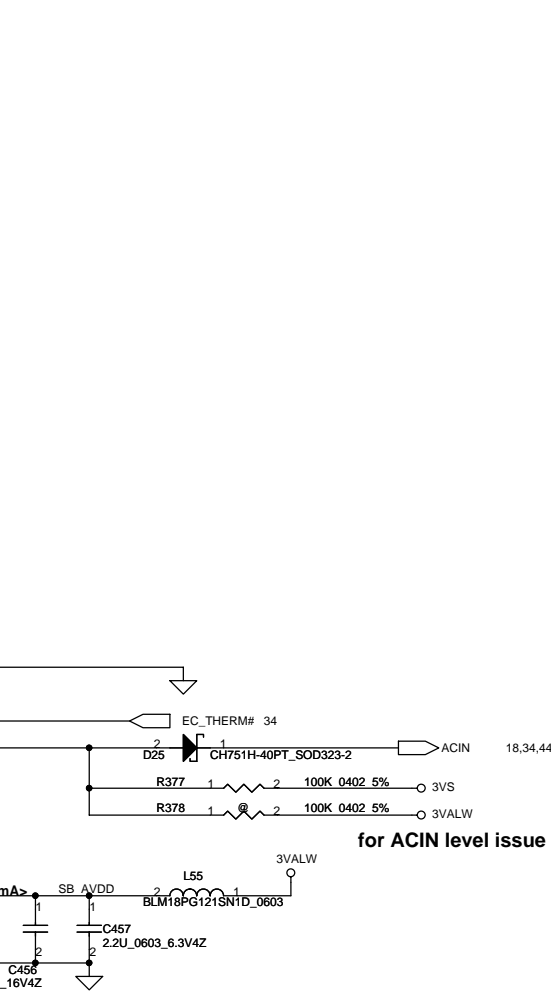
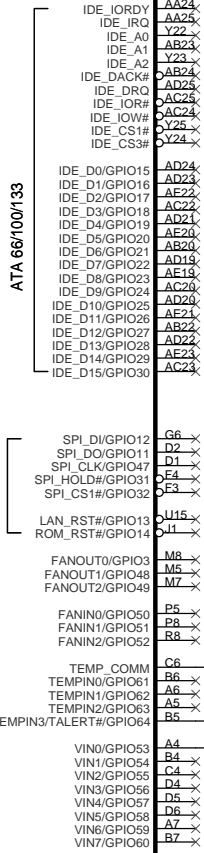
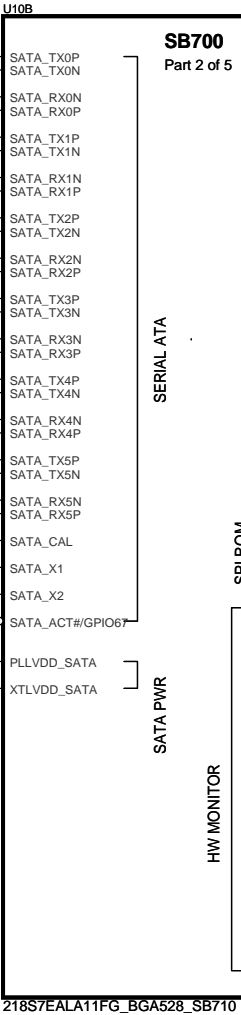
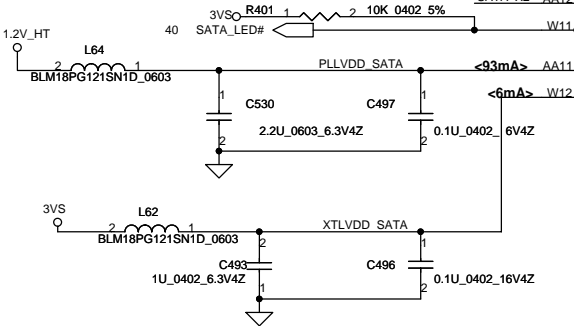
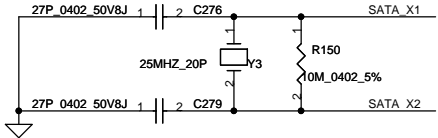
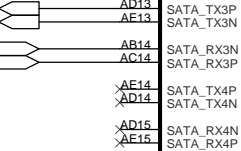
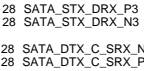
Main  
HDD



Main  
ODD



2nd  
ODD



for ACIN level issue

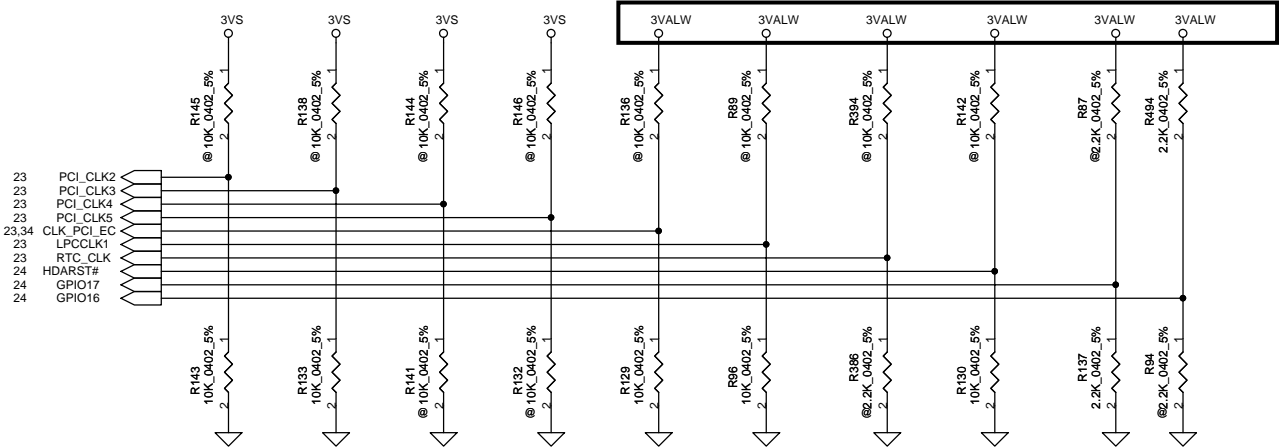
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

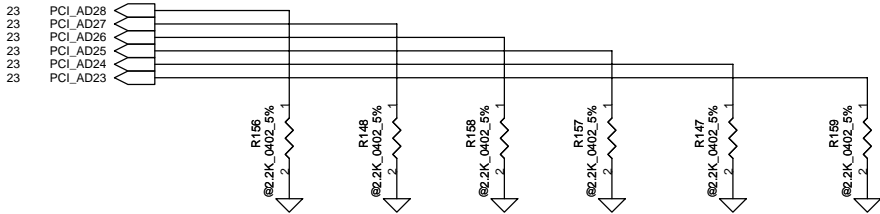
PULL	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved  H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT  DEFAULT	CLKGEN DISABLED  DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		

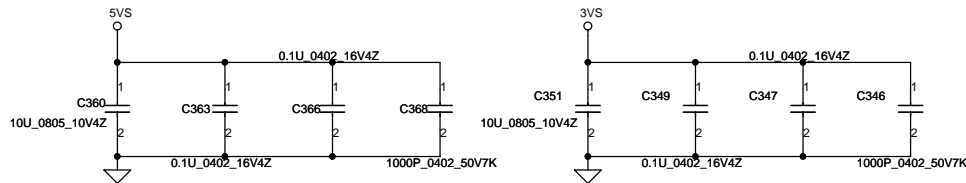


DEBUG STRAPS

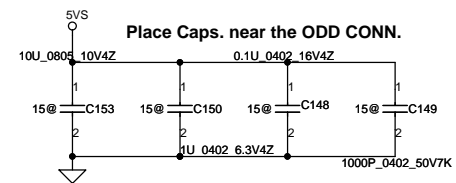
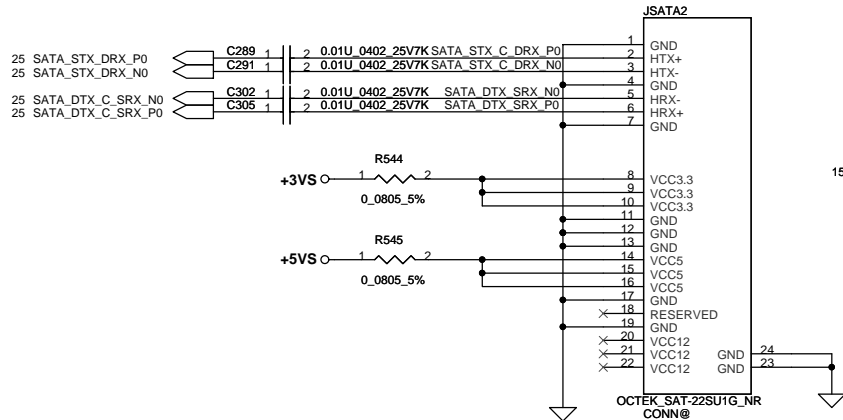
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL  DEFAULT	USE ACPI BCLK  DEFAULT	USE IDE PLL  DEFAULT	USE DEFAULT PCIE STRAPS  DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

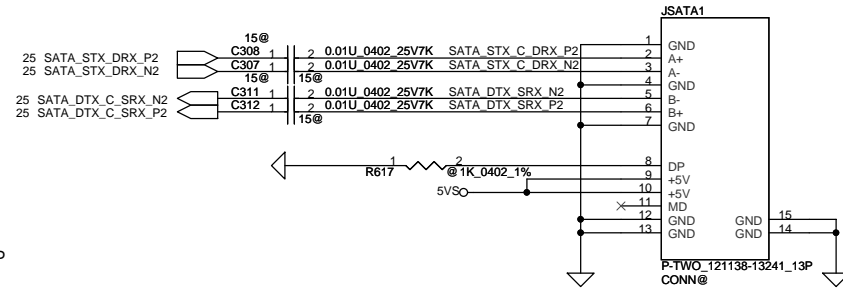




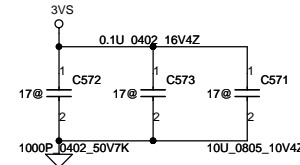
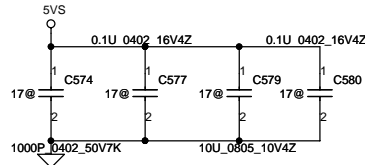
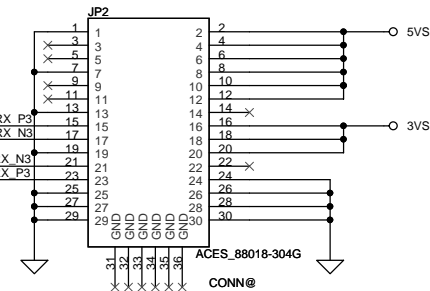
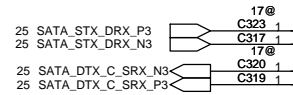
## SATA HDD CONN



## SATA ODD CONN

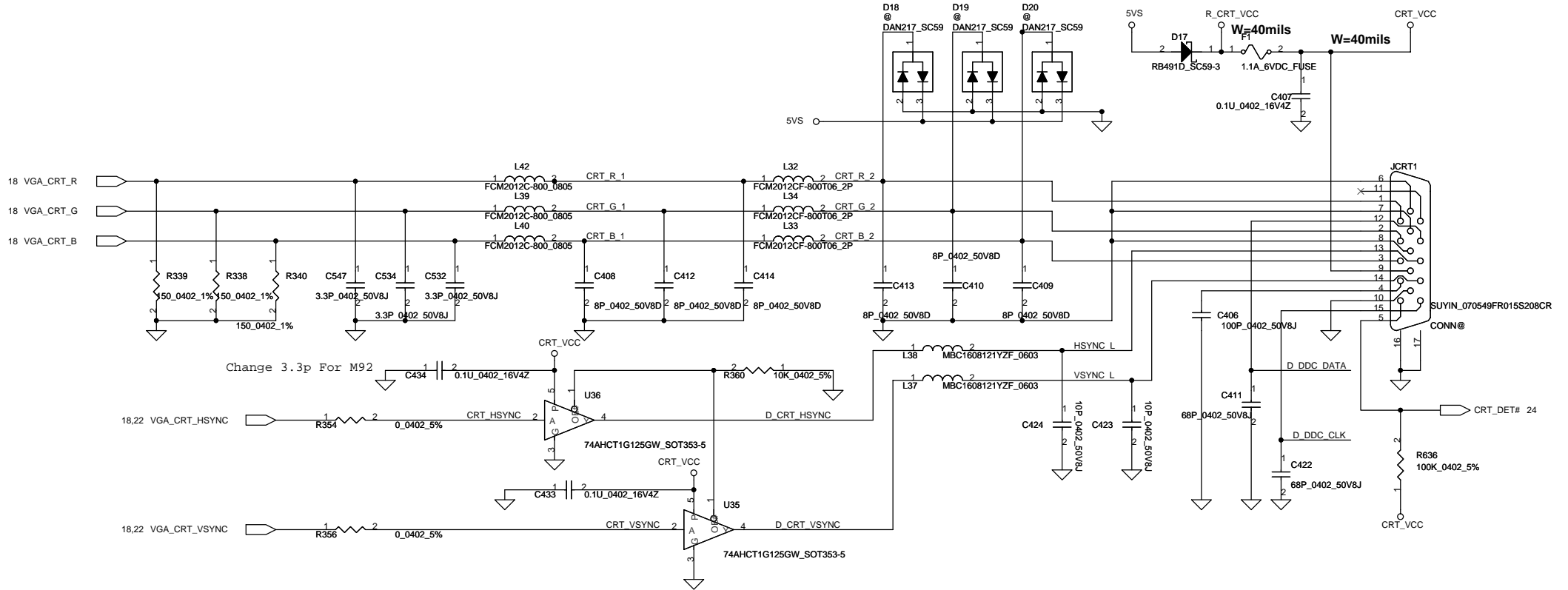


## Second ODD

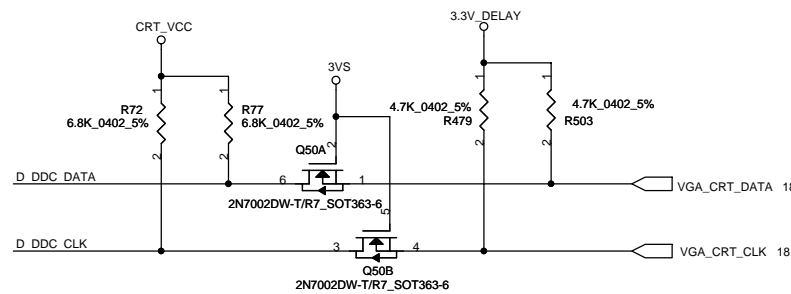


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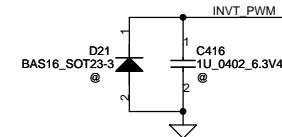
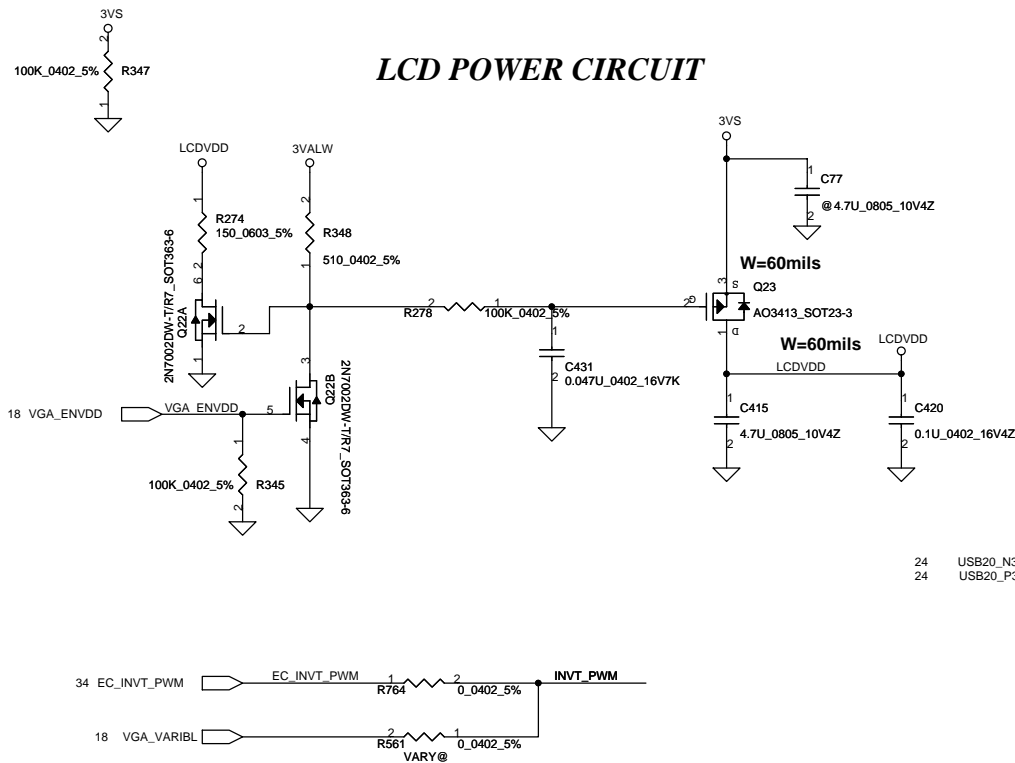
# CRT Connector



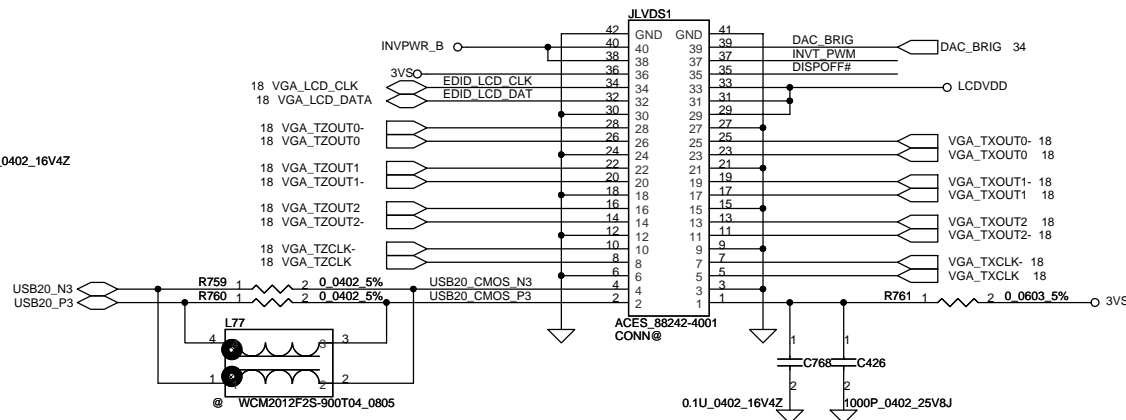
## Close to Conn side

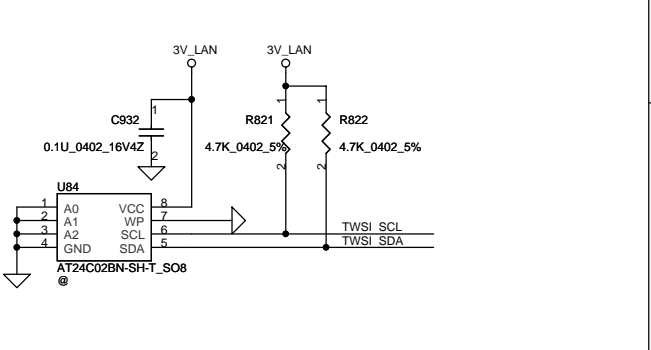
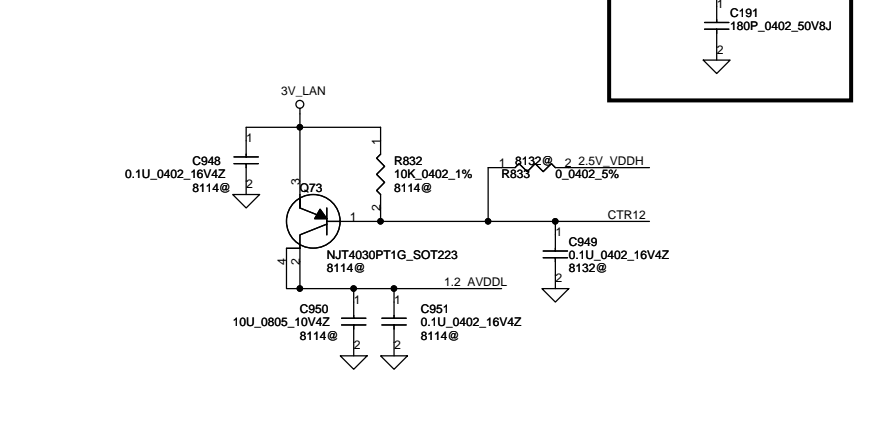
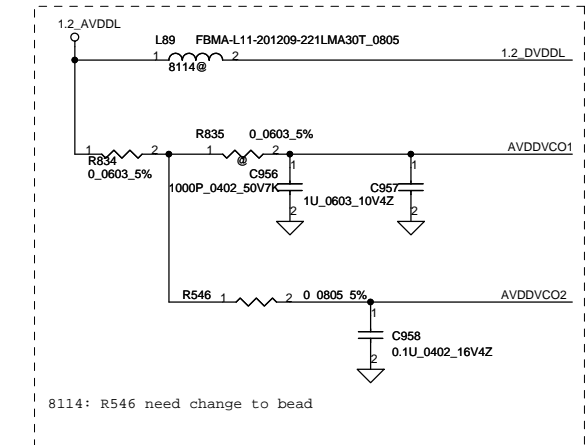
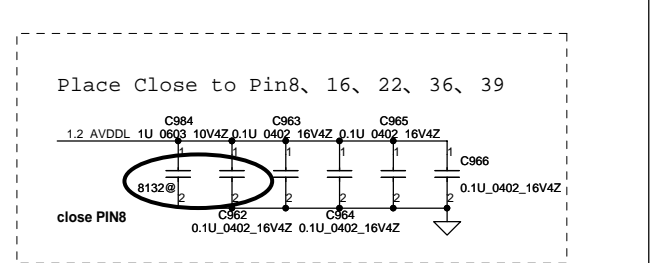
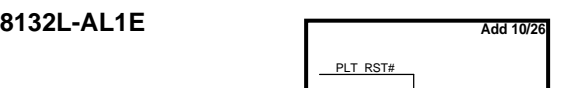
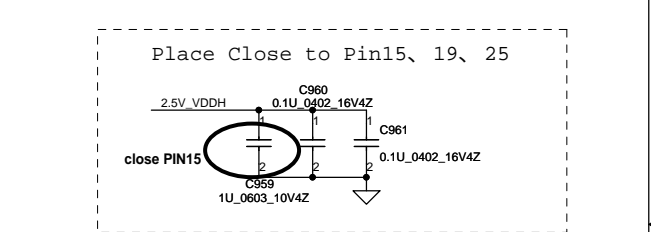
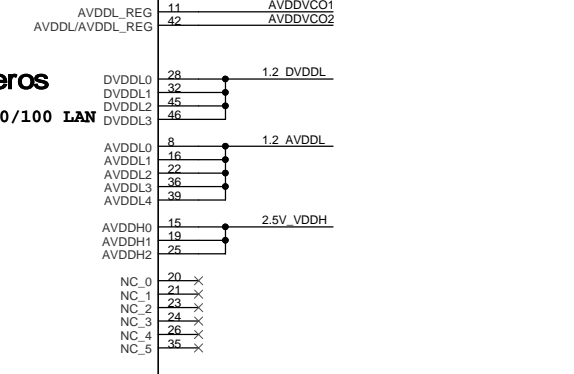
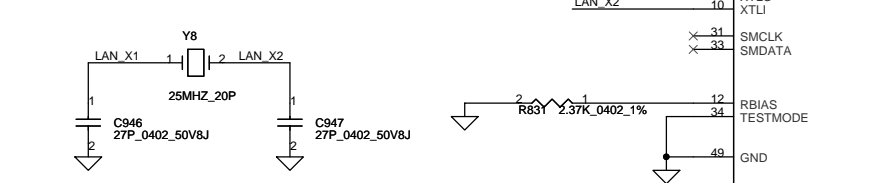
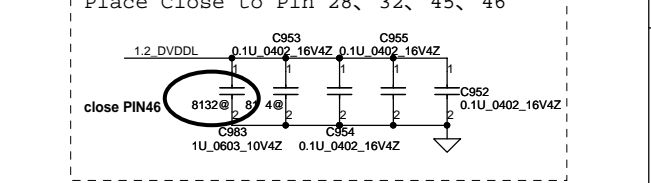
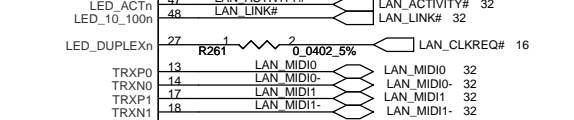
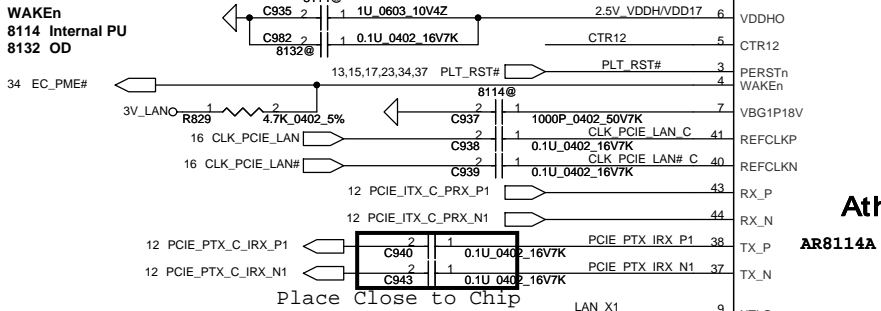
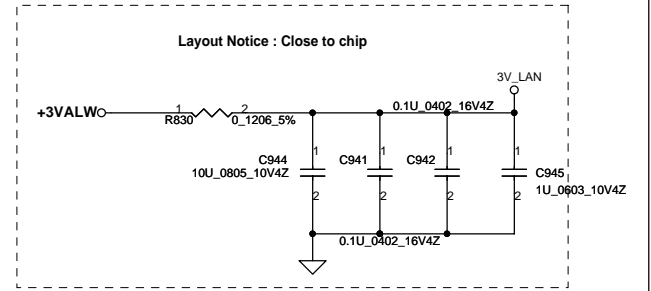
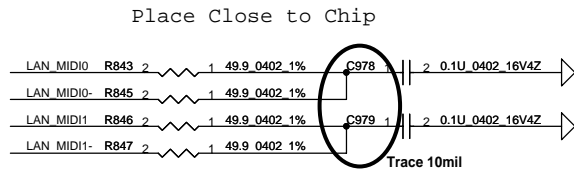
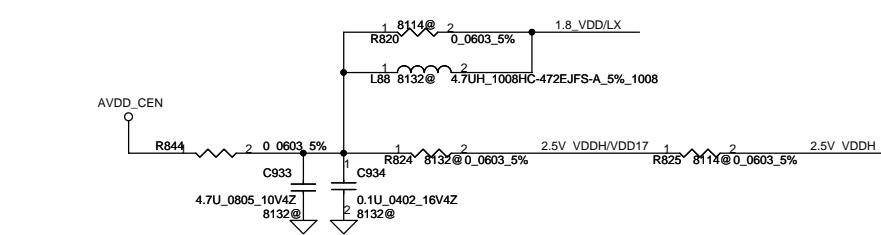


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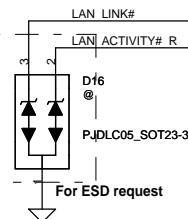
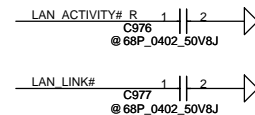


### LCD/PANEL CONN.



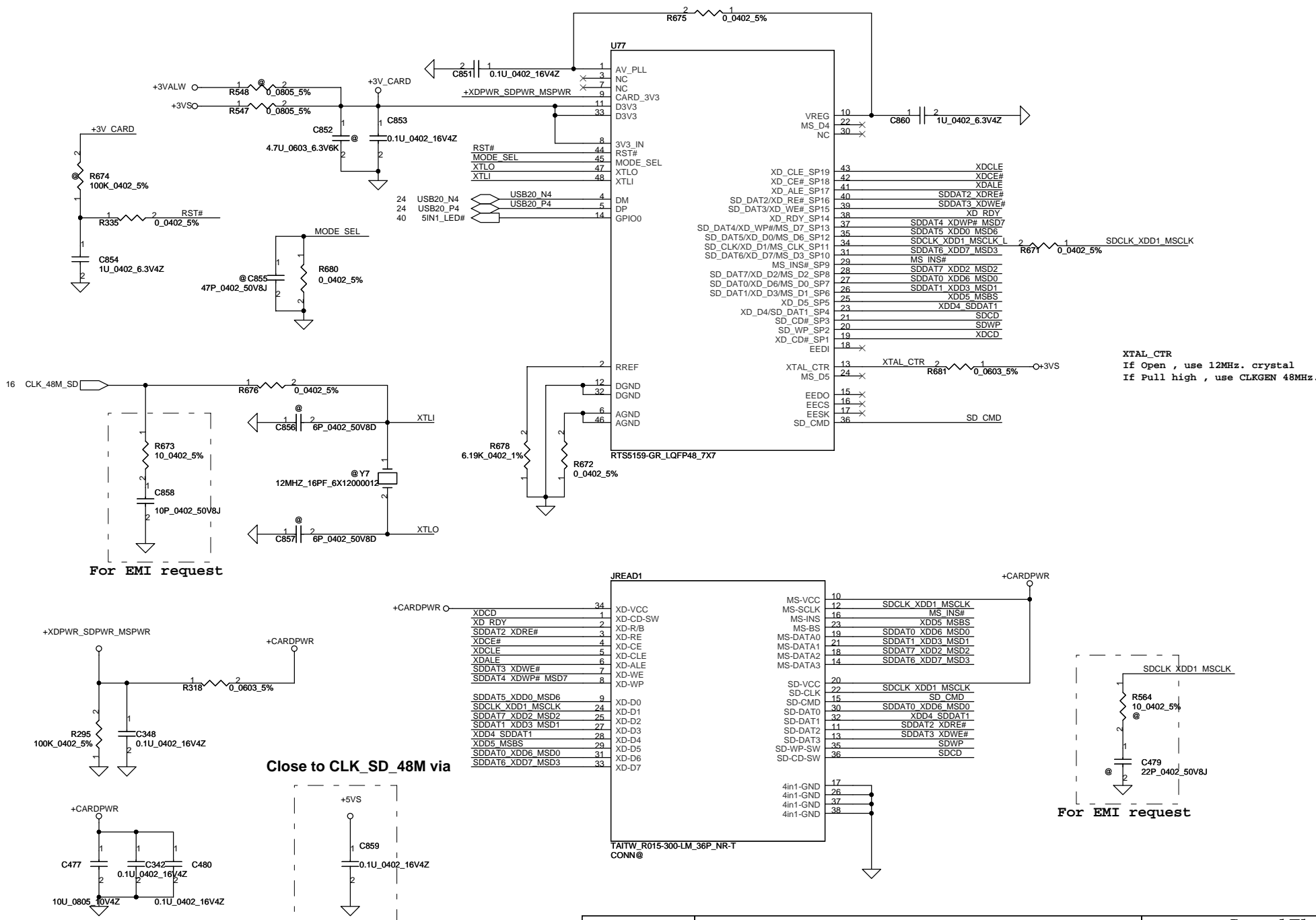


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XTAL\_CTR  
If Open , use 12MHz. crystal  
If Pull high , use CLKGEN 48MHz.

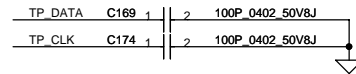
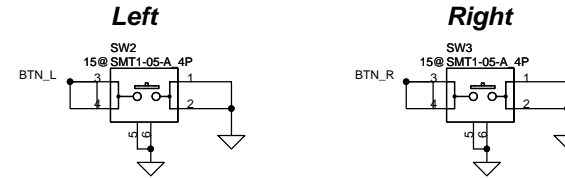
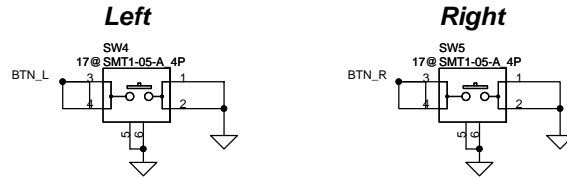
For EMI request

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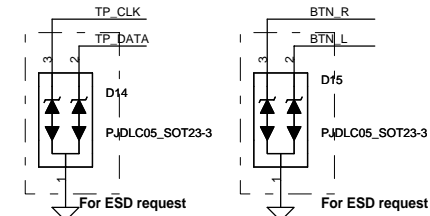
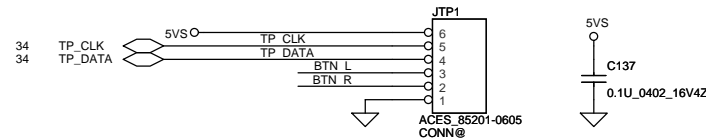


For 17"

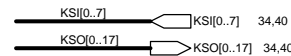
For 15"



TP/B Conn.

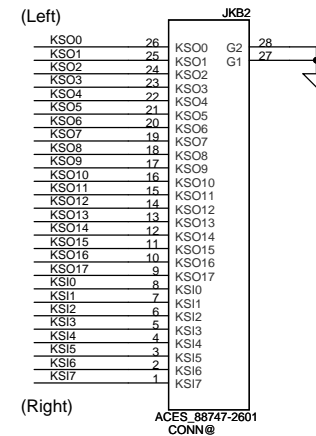
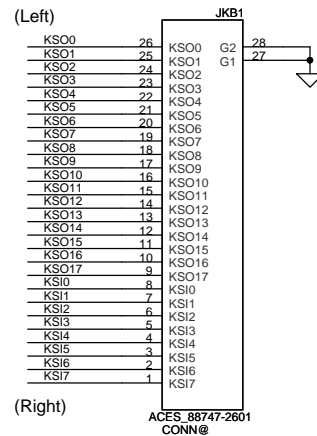
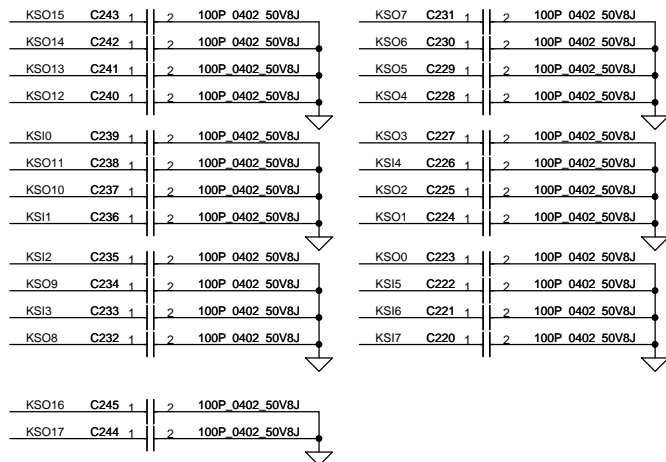


Change to SCA00000200



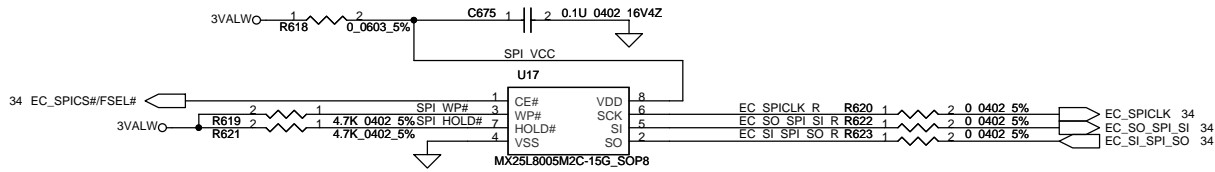
INT\_KBD Conn.

KB1 for 15"  
KB2 for 17"



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***SPI Flash ROM 16M\*1***



SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P

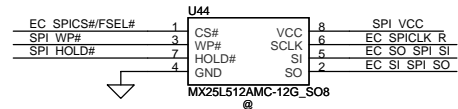
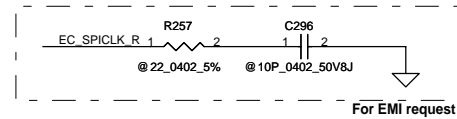
### ENE suggestion SPI Frequency over 66MHz

SST: 50MHz

MXIC: 70MHz

ST: 40MHz

**ONLY MXIC used in this project (66MHz)**

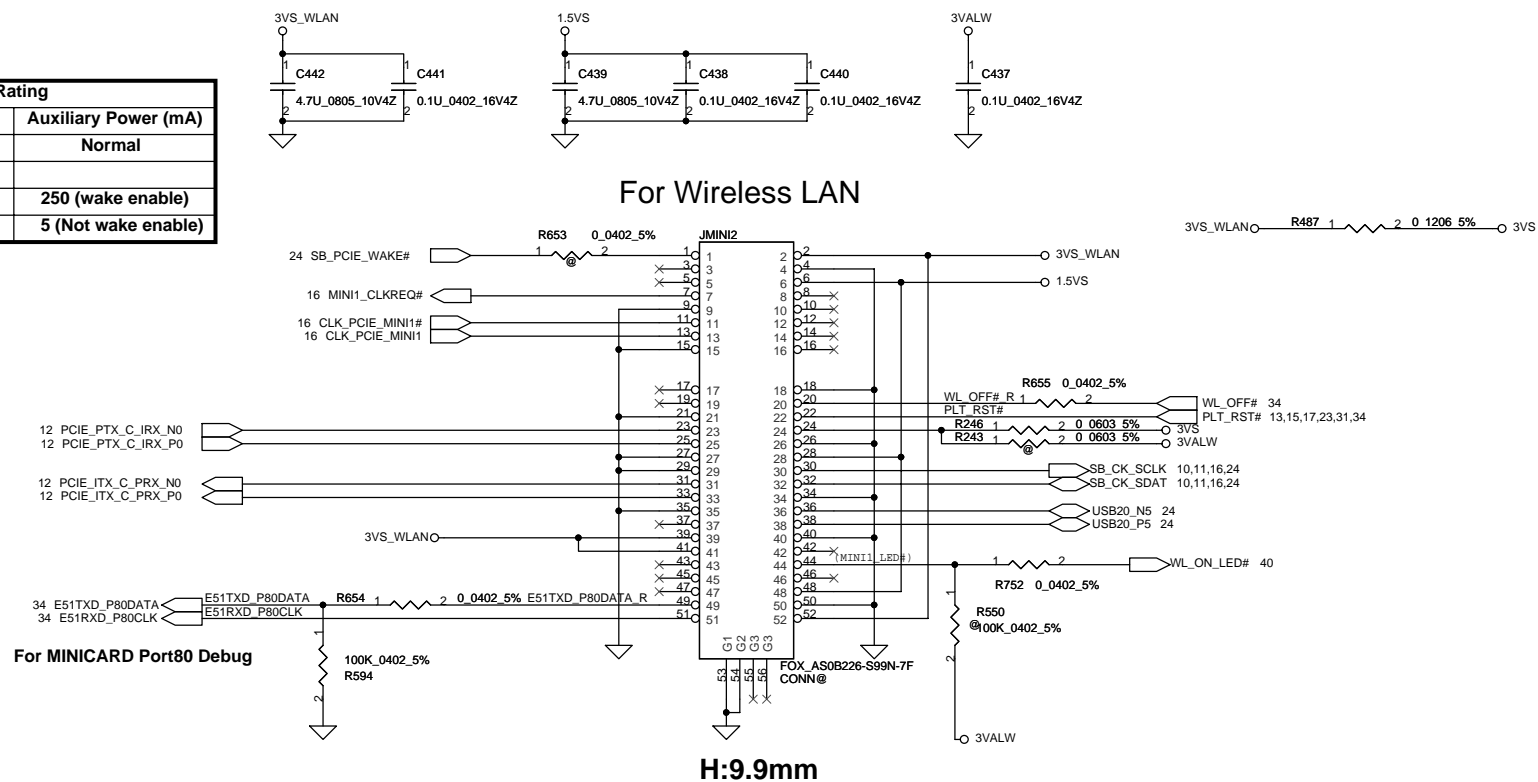


Reserved for BIOS simulator.  
Footprint SO8

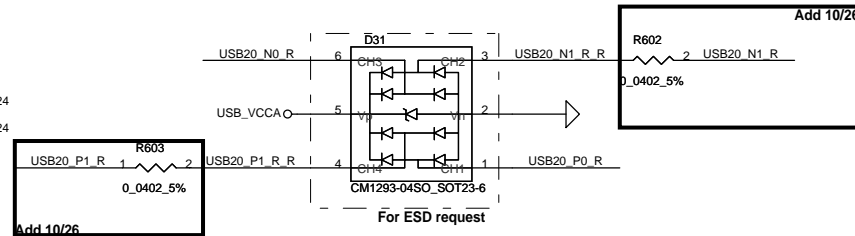
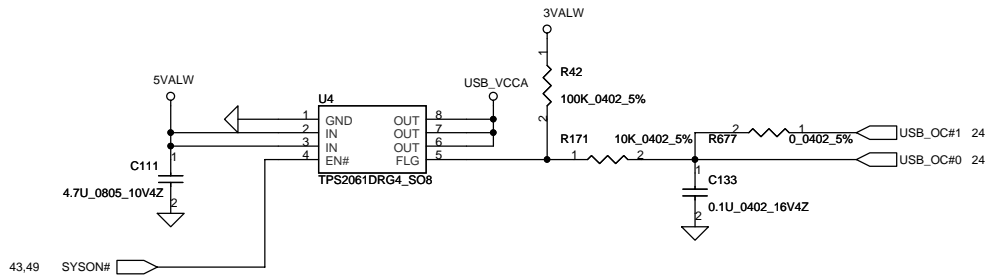
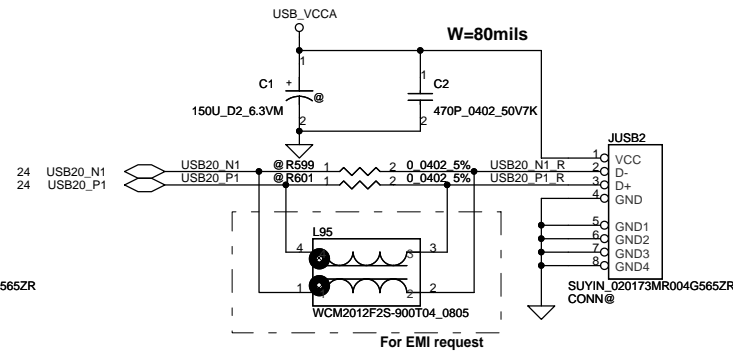
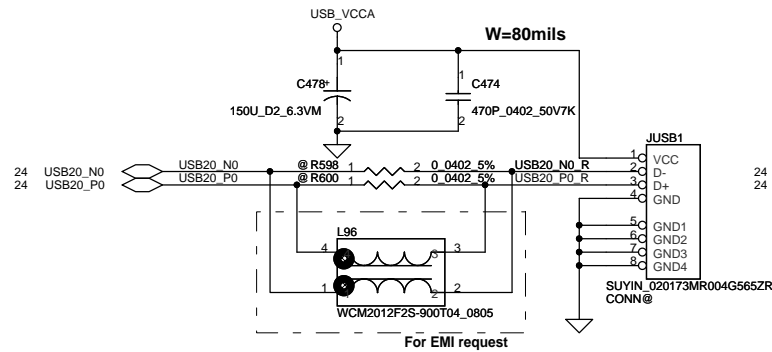
**SPI ROM Footprint 150mil**

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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



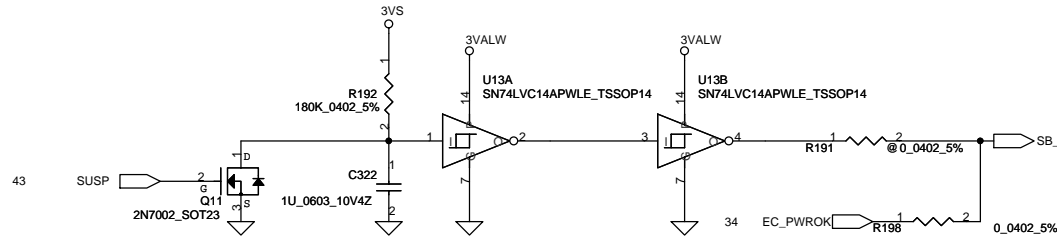
# USB CONN. 1 & 2



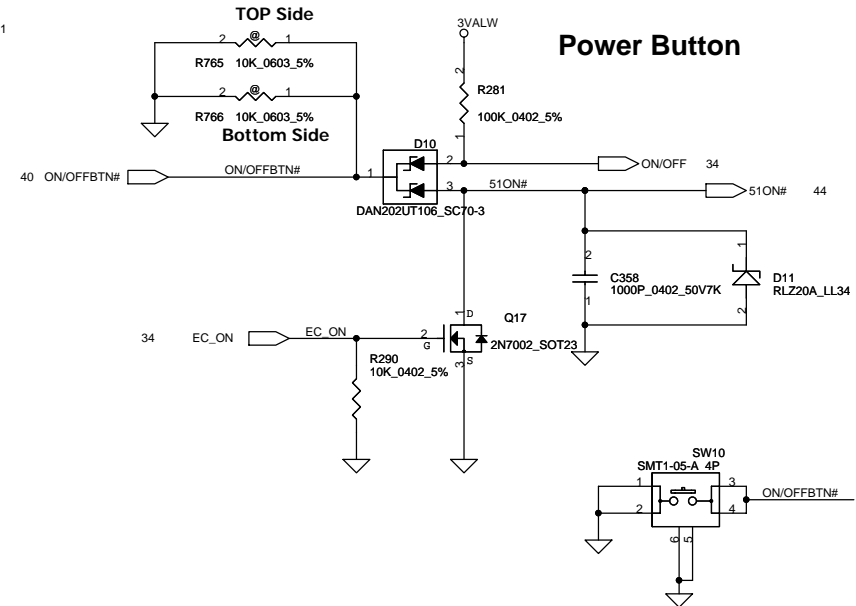
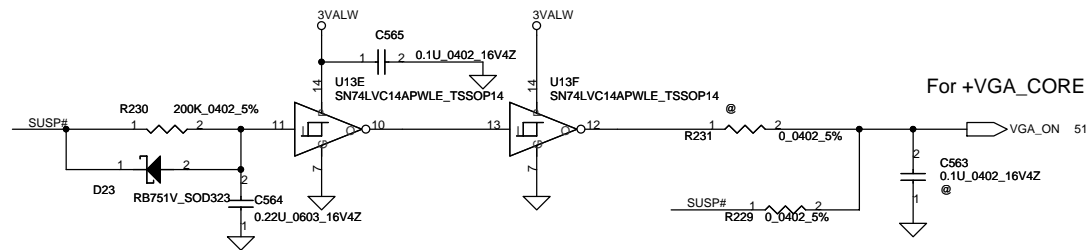
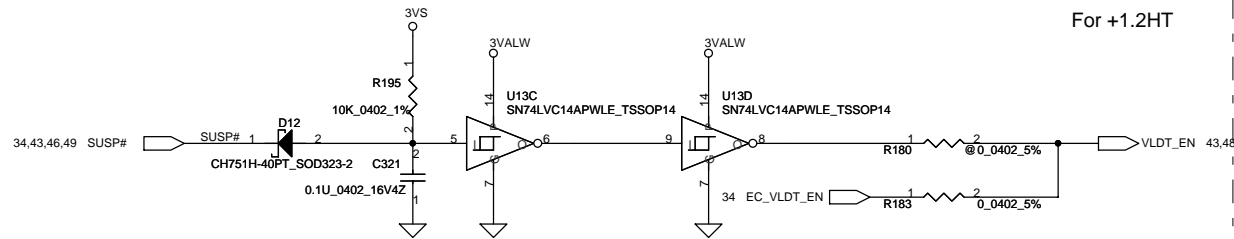
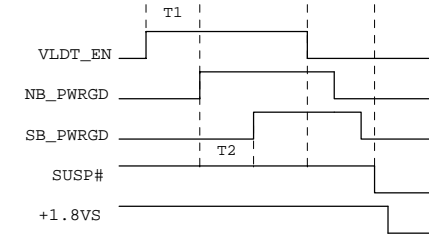
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## Power ON Circuit

For South Bridge

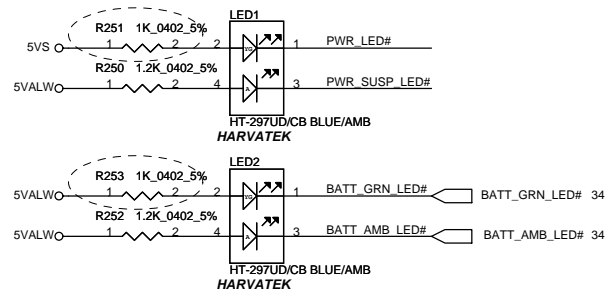
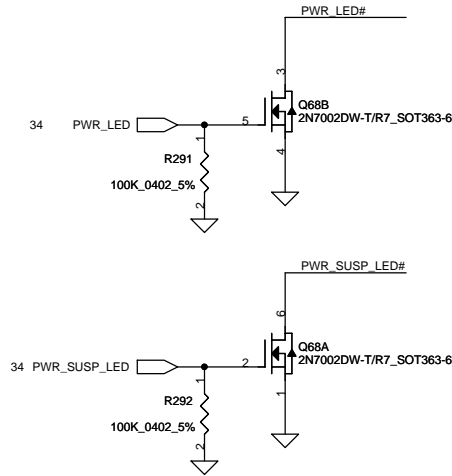


note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,  
SUSP# goes to low after SB\_PWRGD goes to low for power down.

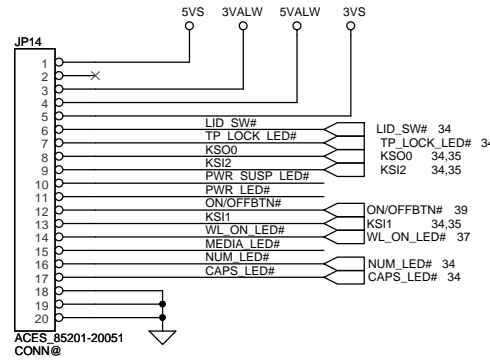


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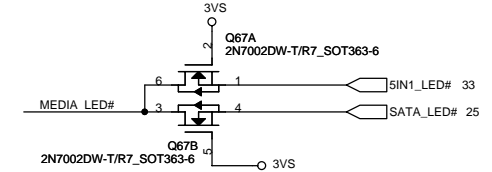
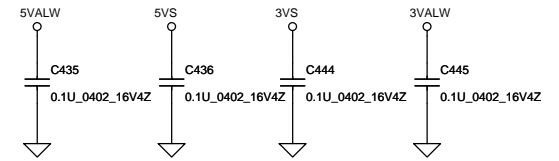
## To PWR LED/B



## BLUE/AMB LED



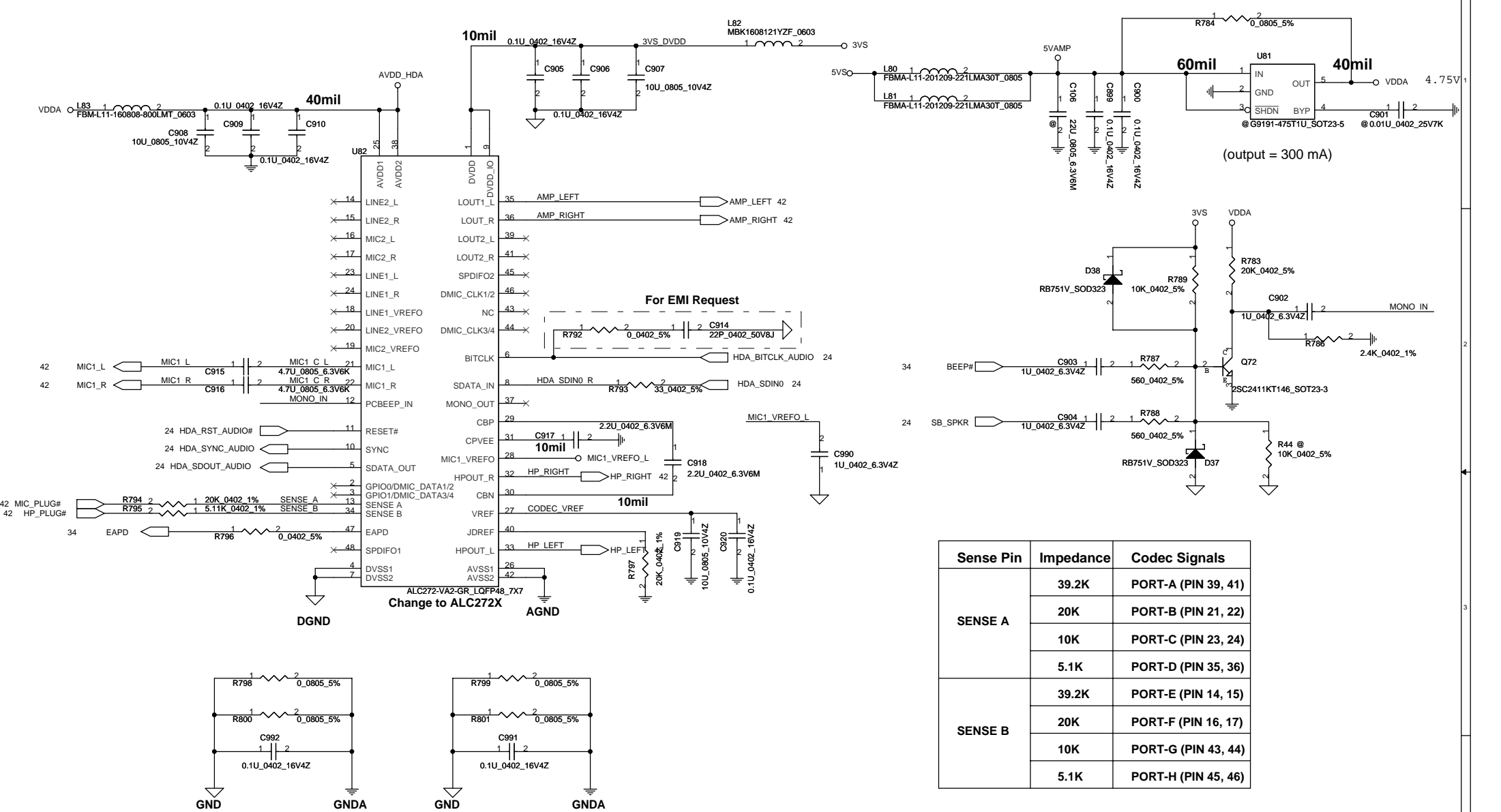
	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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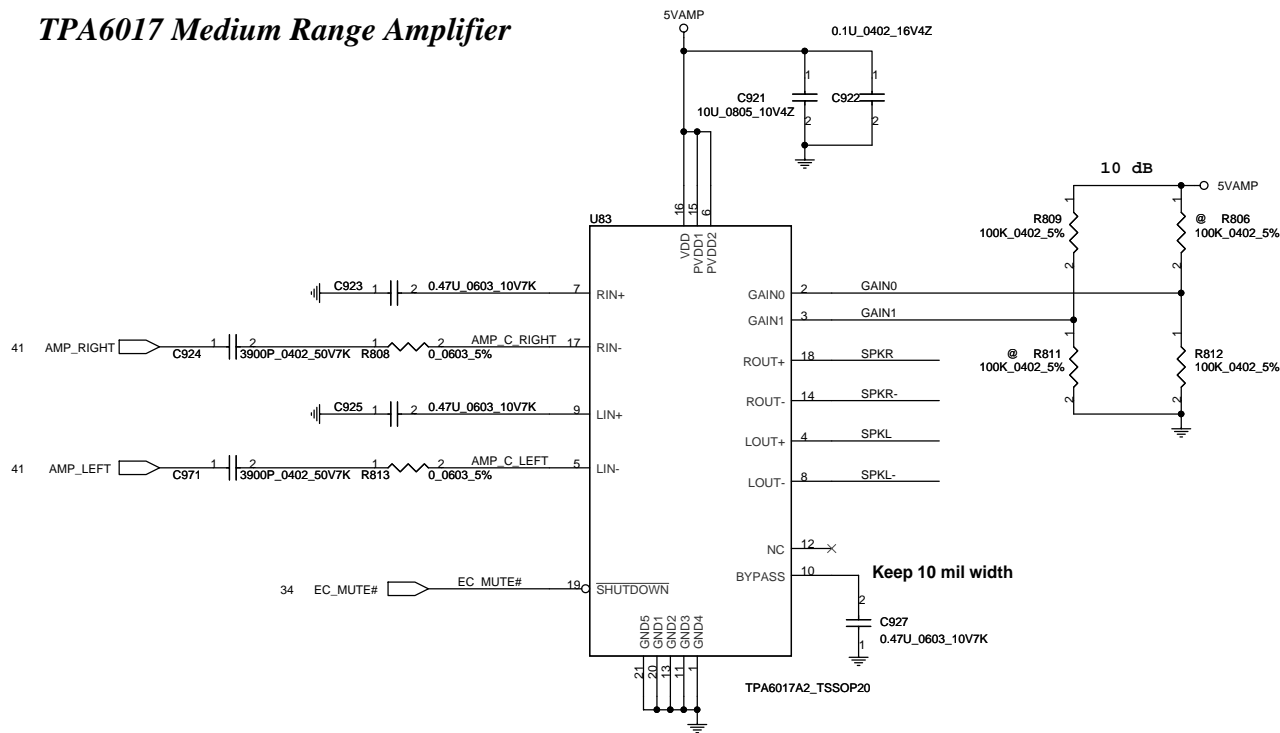


HD Audio Codec

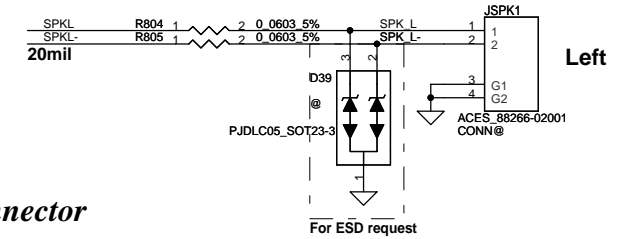


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

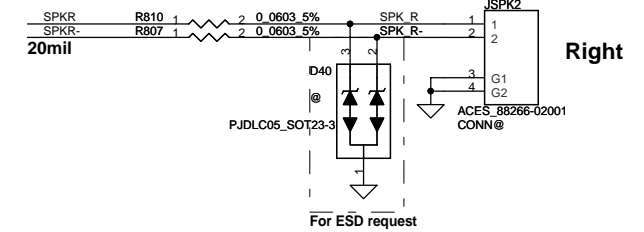
# TPA6017 Medium Range Amplifier



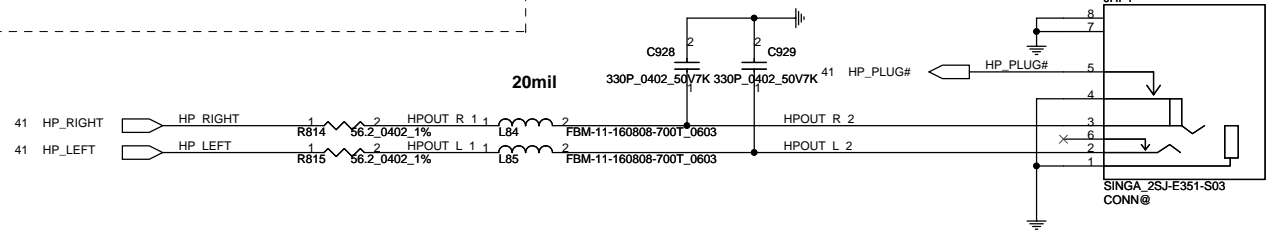
## Left Connector



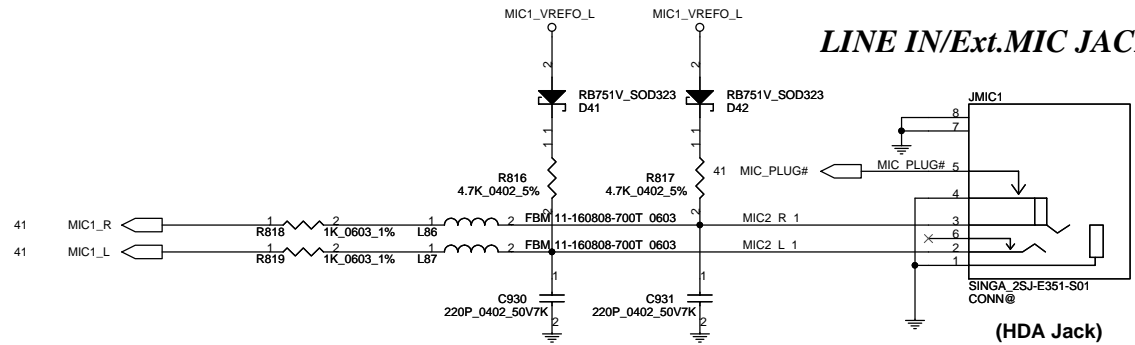
## Right Connector



## LINE Out/Headphone Out



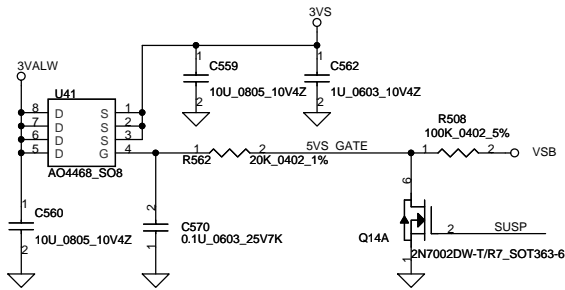
## LINE IN/Ext.MIC JACK



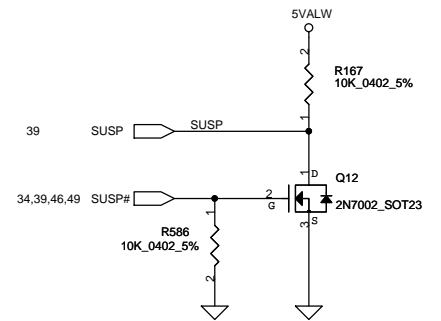
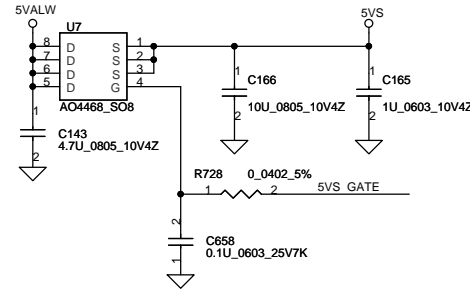
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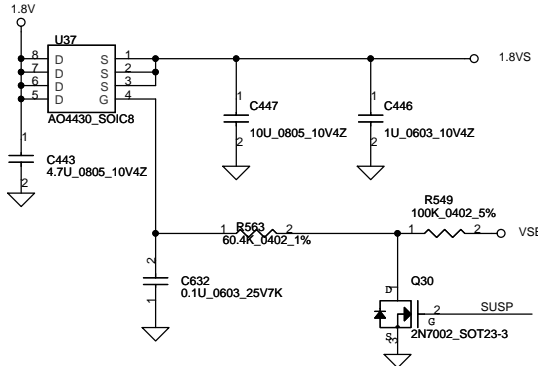
### +3VALW TO +3VS



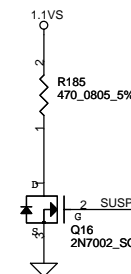
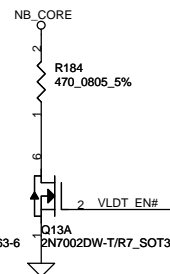
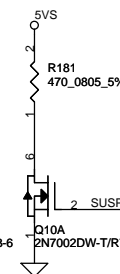
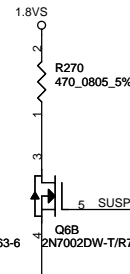
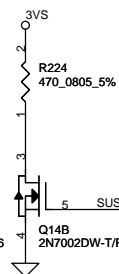
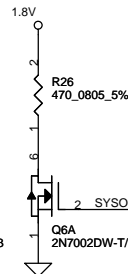
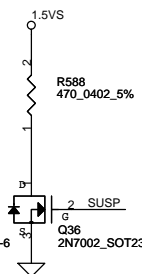
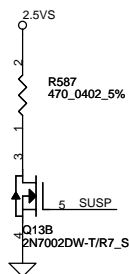
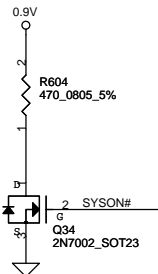
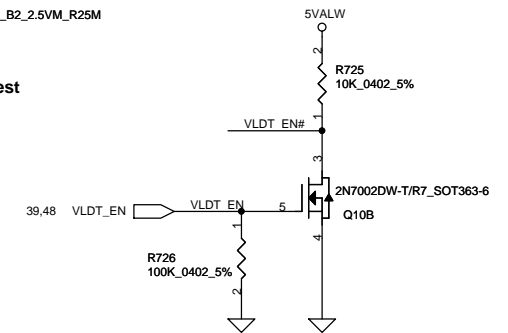
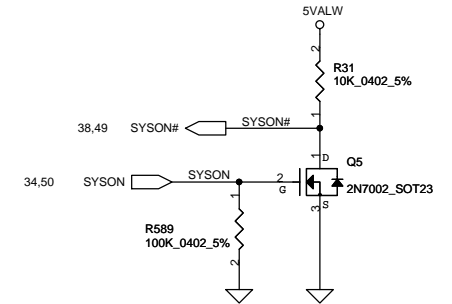
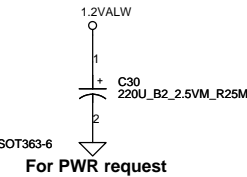
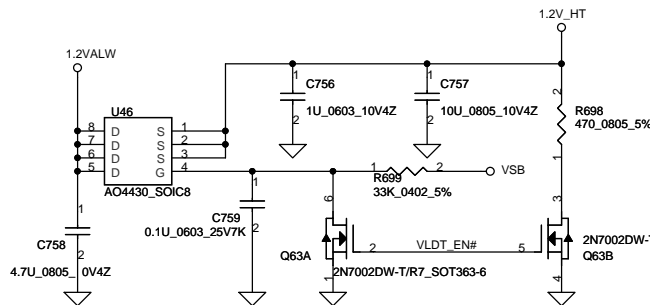
### +5VALW TO +5VS



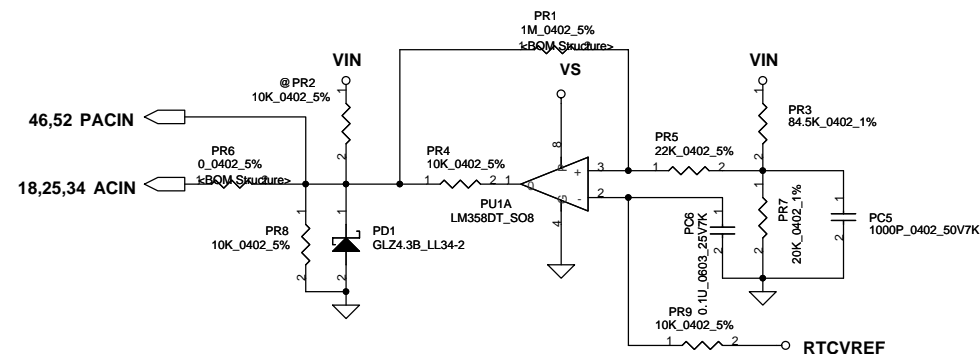
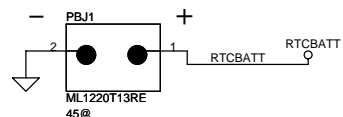
### +1.8V TO +1.8VS



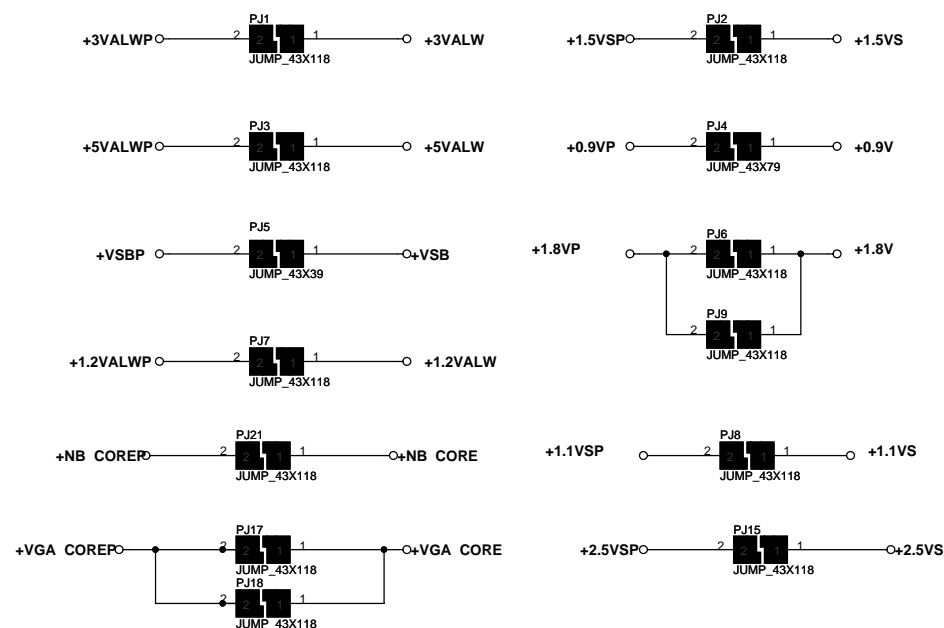
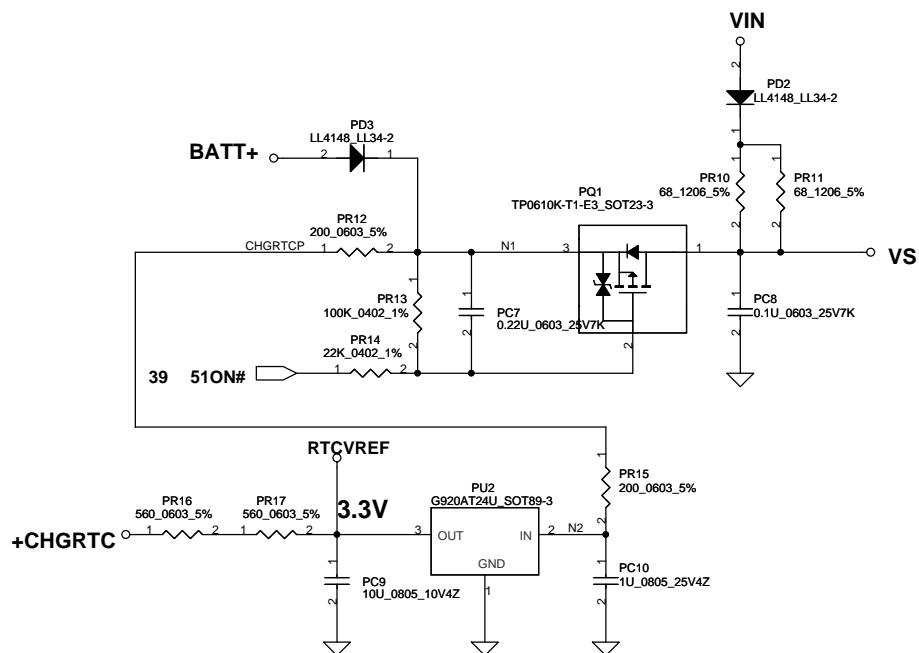
### +1.2VALW TO +1.2V\_HT



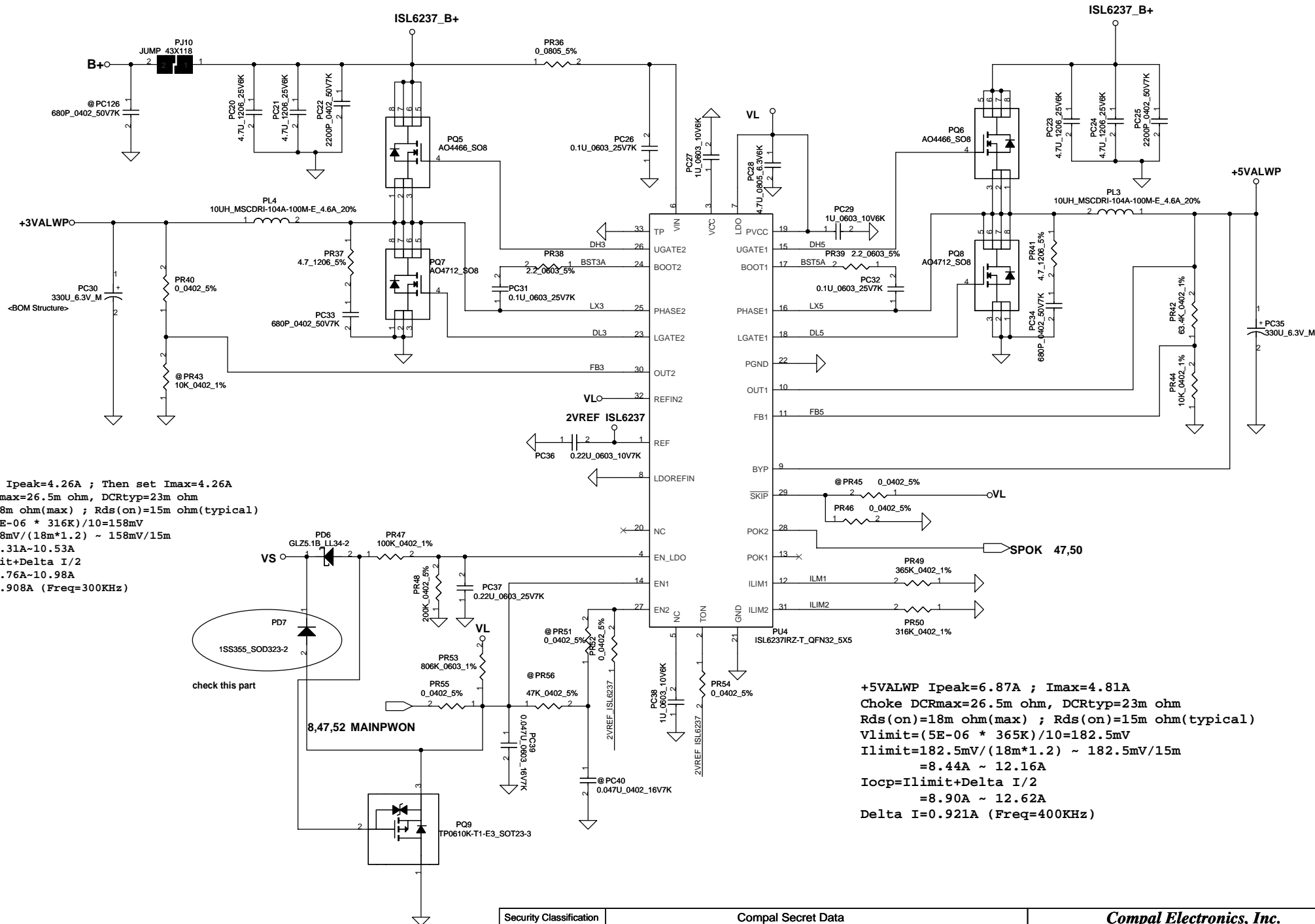
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Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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+3.3VALWP Ipeak=4.26A ; Then set I<sub>max</sub>=4.26A  
 Choke DCR<sub>max</sub>=26.5m ohm, DCR<sub>typ</sub>=23m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 316K)/10=158mV  
 I<sub>limit</sub>=158mV/(18m\*1.2) ~ 158mV/15m  
 =7.31A~10.53A  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =7.76A~10.98A  
 Delta I=0.908A (Freq=300KHz)

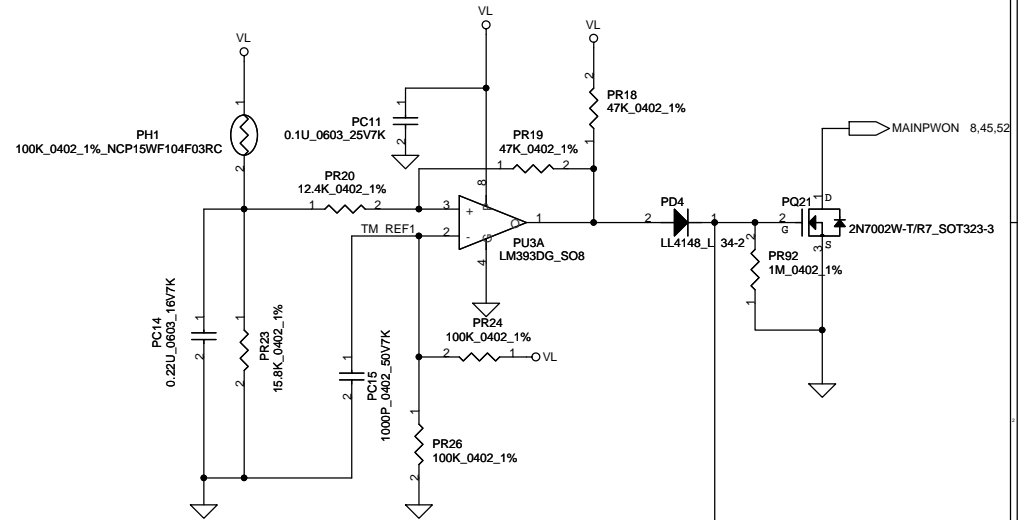
+5VALWP Ipeak=6.87A ; I<sub>max</sub>=4.81A  
 Choke DCR<sub>max</sub>=26.5m ohm, DCR<sub>typ</sub>=23m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 365K)/10=182.5mV  
 I<sub>limit</sub>=182.5mV/(18m\*1.2) ~ 182.5mV/15m  
 =8.44A ~ 12.16A  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =8.90A ~ 12.62A  
 Delta I=0.921A (Freq=400KHz)

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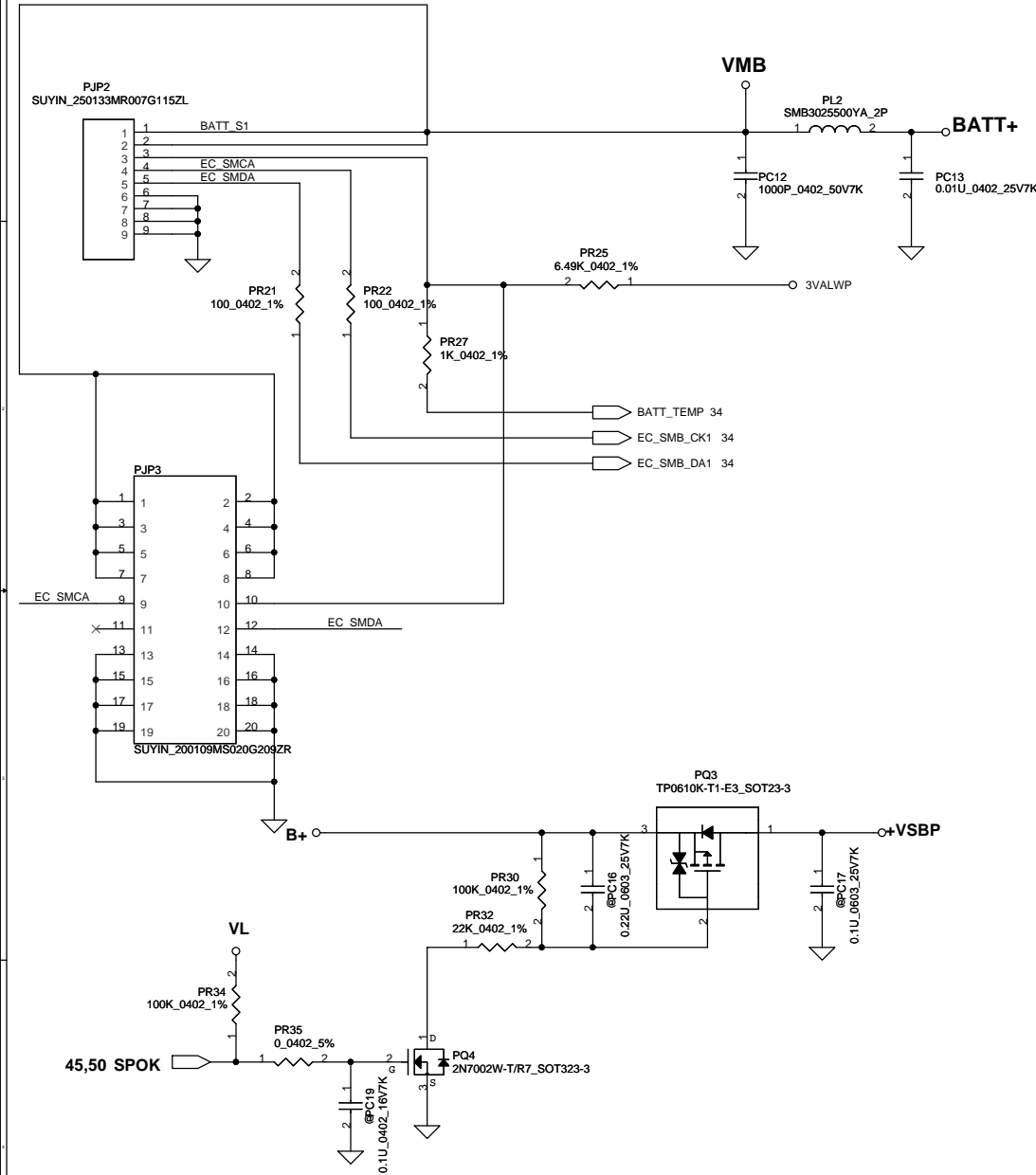
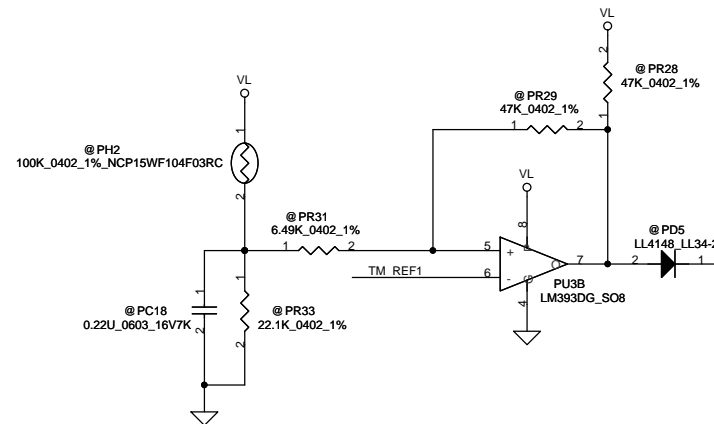


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PH1 under CPU botten side :  
CPU thermal protection at 92 degree C



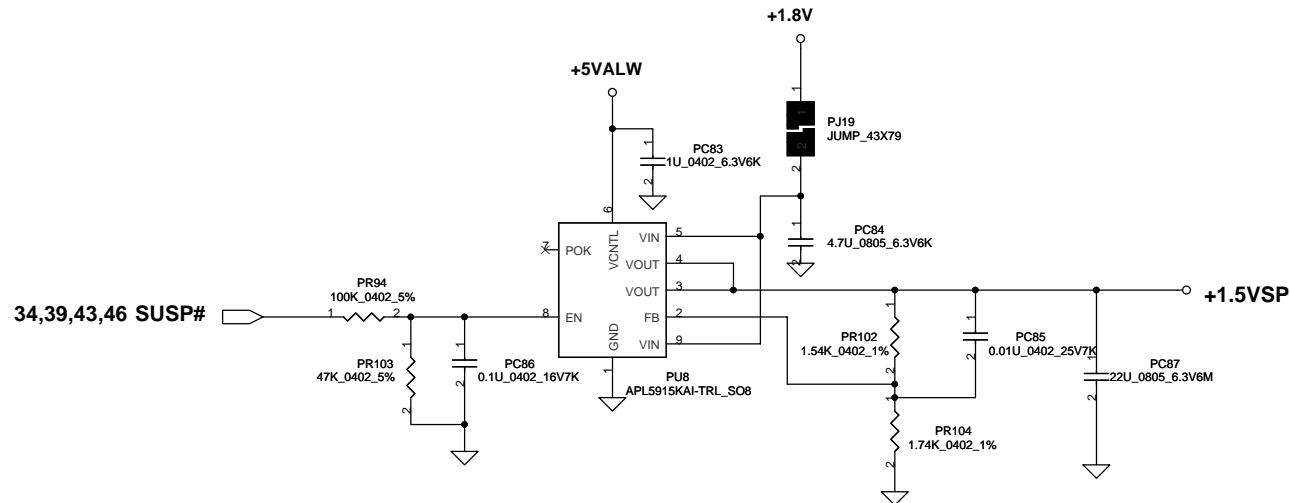
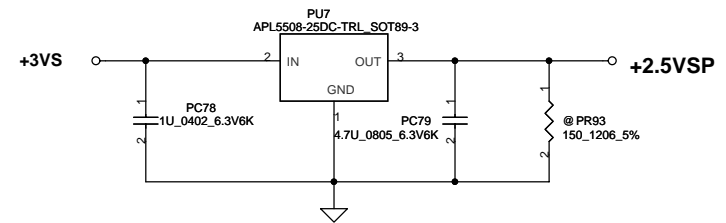
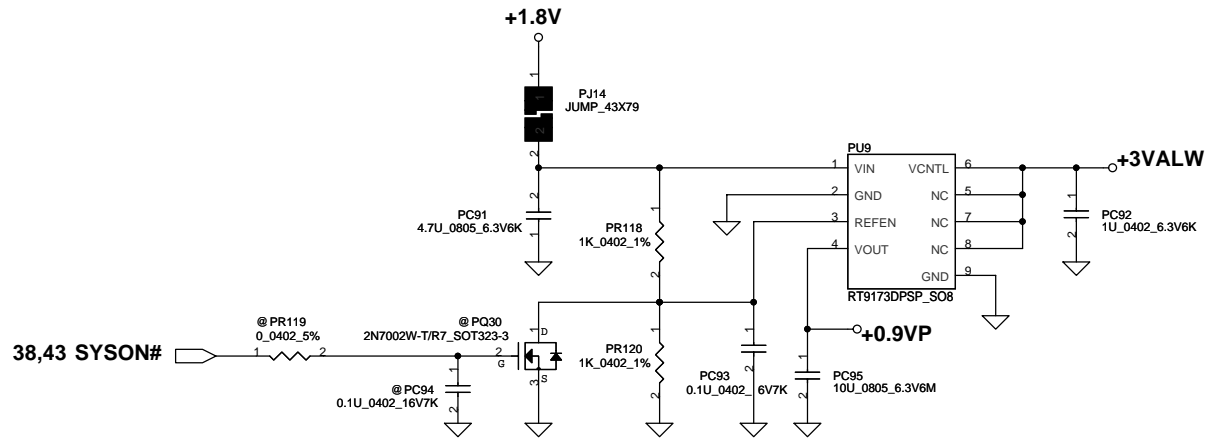
PH2 near main Battery CONN :  
BAT. thermal protection at 75 degree C



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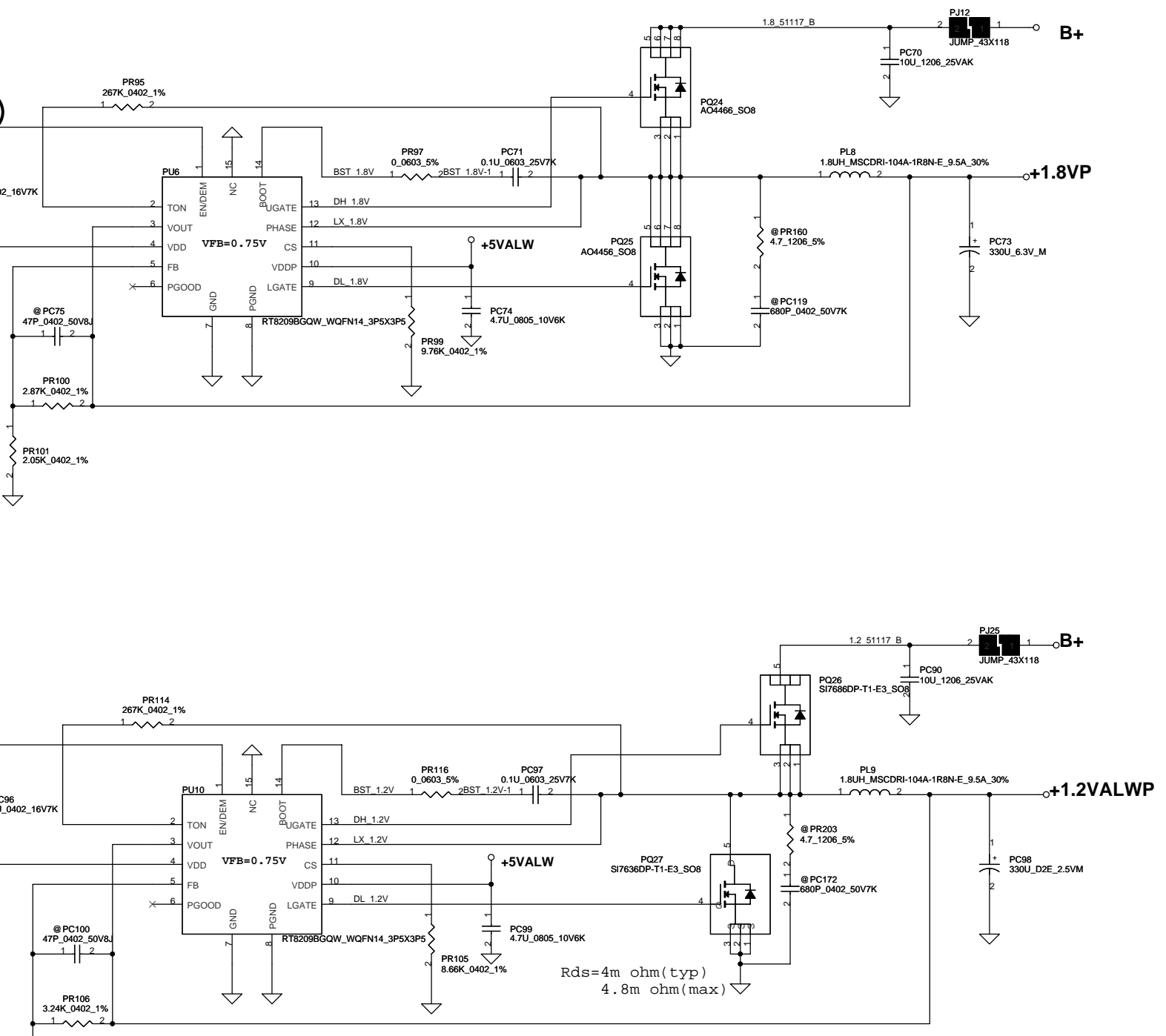
VFB=0.75V  
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$   
 $R_{ton} = 267K \Rightarrow F_{aw} = 297KHz$

Cout ESR=15m ohm  
 $I_{peak} = 11.96A$ ,  $I_{max} = 8.372A$   
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$   
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$   
 $\Rightarrow 1/2 \Delta I = 1.524A$   
 $R_{trip} = 9.76K$   
 $I_{ocp} = 15.20A - 24.71A$

VFB=0.75V  
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$   
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

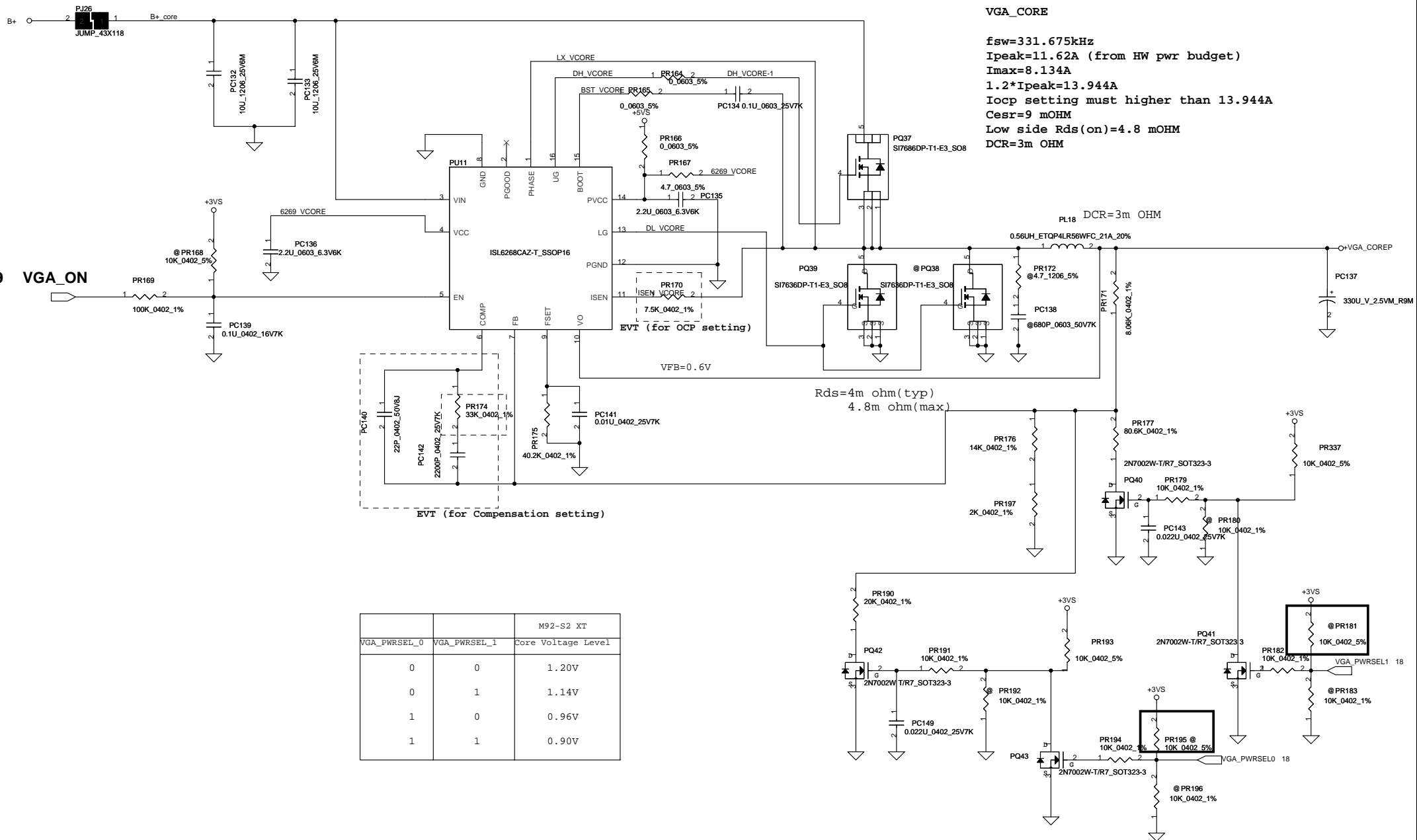
1.2VP  $I_{peak} = 7.4A$  ;  $I_{max} = 5.180A$   
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$   
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$   
 $\Rightarrow 1/2 \Delta I = 1.05A$   
 $R_{ds(on)} = 15m / 18m \text{ ohm}$   
 $set R_{trip} = 8.66K$   
 $I_{cop\_min} = 4.77A$   
 $I_{cop\_max} = 7.74A$

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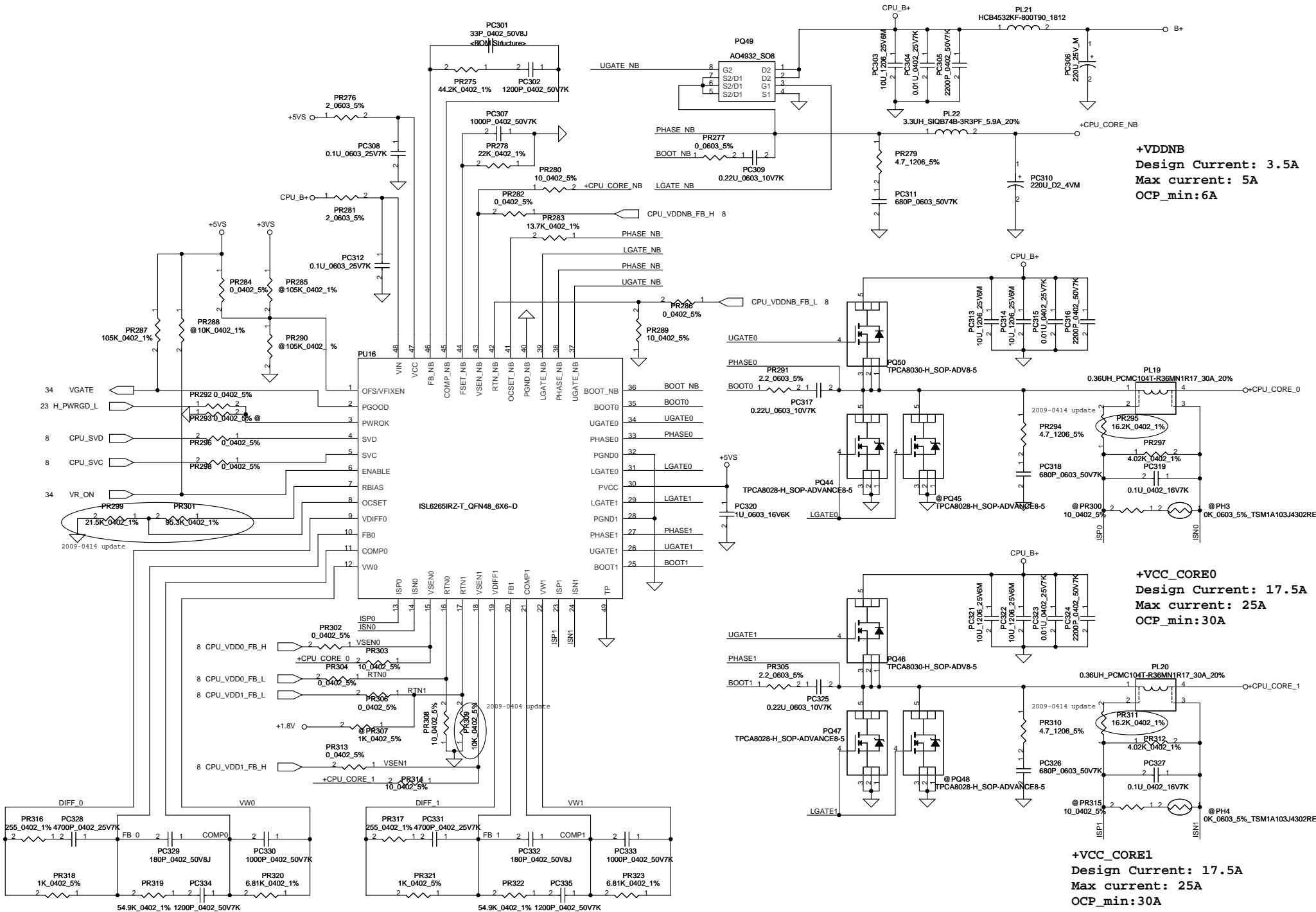
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# 39 VGA\_ON



		M92-S2 XT
VGA_PWRSEL_0	VGA_PWRSEL_1	Core Voltage Level
0	0	1.20V
0	1	1.14V
1	0	0.96V
1	1	0.90V





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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGAI9331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8	Change Power Source	For WLAN wakeup	1.0	37	Change R550 to +3VALW	09, 05/07	Pre-MP
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

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Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P 18	4/9	27				
3	BOM change	Change R178 R179 to 90 9/158 ohm	P 16	4/9	28				
4	BOM change	R30 R39 reserve	P 24	4/9	29				
5	BOM change	Add C30	P 38	4/9	30				
6	BOM change	Add R634 R639	P 28	4/9	31				
7	BOM change	C383 Reserve	P 24	4/9	32				
8		Pop R419	P 20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1 D2 Reserve pop R763	P 24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P 24	5/18					
12	Lid_SW intial issue	Add R19	P 28	5/18					
13	HPET timer issue	Change C288 C290 to 33P	P 16	5/18					
14	BOM change	change C276 C279 10P to 27P	P 19	5/19					
15									
16									
17									
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